BANDPASS ELECTROMECHANICAL SIGMA-DELTA MODULATOR

YU RUI

(M. Eng., Harbin Institute of Technology)

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SUMMARY

Bandpass sigma-delta modulators (ΣΔMs) have been used to robustly digitize the narrowband intermediate frequency (IF) signals in radio frequency (RF) receivers. IF digitization in RF receivers has several important advantages, such as the absence of flicker noise and DC offset. Most of the bandpass ΣΔMs in the literature are implemented with discrete-time circuits, such as switched-capacitor circuits. Due to the limited bandwidth of opamps and other non-idealities at high frequency, this kind of ΣΔMs is not suitable for digitalization at high IF. While continuous-time bandpass ΣΔMs based on active-RC, transconductor-capacitor (Gm-C), and integrated LC resonators can operate at high sampling speed, their performance may be degraded due to some limitations in the resonator or loop filter, such as low quality factor, poor linearity and the need for frequency tuning.

In this thesis, continuous-time bandpass ΣΔMs based on electromechanical resonators and filters are studied. Compared with the loop filters realized with active-RC, Gm-C and LC resonators, the electromechanical resonator has the advantage of high Q factor, wide resonant frequency range and accurate resonant frequency without the need for automatic tuning. A novel anti-resonance cancellation and a phase delay compensation techniques are proposed to obtain the desired resonator transfer function. Both 2^{nd}- and 4^{th}-order ΣΔMs are successfully implemented in a standard 0.35-μm CMOS technology and tested with various electromechanical resonators, including the SAW resonators with resonant frequencies of 47.3MHz, 77.25MHz, and 108.9MHz, and

a 19.6-MHz silicon MEMS resonator. The measurement results of the 2nd-order ΣΔM indicate that such modulator can achieve superior performance compared with traditional discrete-time and continuous-time 2nd-order ΣΔMs. The measurement results of the 4th-order ΣΔM based on two SAW resonators, however, show large degradation from the simulation result, which may be attributed to the imperfect anti-resonance cancellation. The measured peak SNDRs for the 47.3-MHz SAW resonator and 19.6-MHz MEMS resonator based 2nd-order ΣΔMs are 54dB and 51dB, respectively. The peak SNDR for the 4th-order 47.3-MHz SAW resonator based ΣΔM is 66dB. All above are measured in a 200-kHz signal bandwidth.

The electromechanical filter based wideband bandpass ΣΔM is also studied. Analysis shows that not all the electromechanical filters can be used to realize the bandpass ΣΔMs. A careful study of the existing electromechanical filters indicates that mechanically-coupled MEMS and longitudinally-coupled SAW filters are two possible candidates. A 4th-order electromechanical filter based bandpass ΣΔM with multi-feedback is proposed and demonstrated using a 110-MHz SAW filter with a passband of 1MHz. The proposed bandpass ΣΔM is successfully implemented in a 0.35-μm SiGe HBT BiCMOS process and achieves the measured peak SNDR of 60dB and dynamic range of 65dB in 1-MHz signal bandwidth. The performance is comparable with most of the existing CMOS/BiCMOS bandpass ΣΔMs.

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CHAPTER 1

INTRODUCTION

Wireless communication plays an important role in our daily life. Its explosive growth has resulted in the proliferation of many appliances, including cordless telephones, cellular telephones, digital radio receivers, global positioning system (GPS) handled units, and etc. Besides, new technologies and applications, such as Bluetooth, wireless local areas networks (WLANs), software defined radios (SDRs) and ultra wideband (UWB) communication, are continuously emerging. This variety of applications has led to many wireless communication standards. In addition, consumers are demanding low cost, low power and small form factor devices. As a result, recent efforts in the design of integrated wireless radio frequency (RF) transceivers have focused on increased integration level as well as adaptability to multiple RF communication standards [1].

The role of a RF receiver is to extract a desired and possibly weak signal from a wideband frequency spectrum in the presence of strong noise and interference with a specific signal-to-noise ratio (SNR) [2]. In superheterodyne [3] and homodyne [4] receivers, the signal is down-converted to baseband before it is digitized by a lowpass analog-to-digital converter (ADC). Another type of the receiver is shown in Figure 1.1(a), in which the RF signal is converted to an intermediate frequency (IF) and directly digitized at the IF stage. Such a receiver is referred to as IF digitization receiver [5]. A bandpass ADC is therefore required for the IF digitization. The channel filter before the

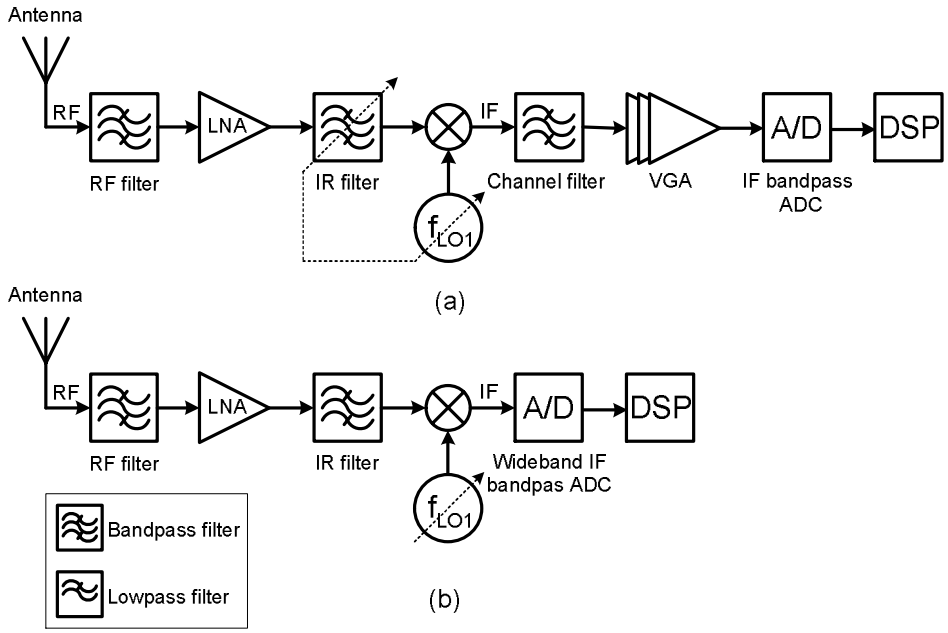


Figure 1.1 IF digitization receiver with (a) narrowband ADC and (b) wideband ADC

ADC preserves the moderate dynamic range, bandwidth, and linearity requirements for the ADC. This architecture is advantageous for several reasons. First, this receiver is insensitive to DC offset and flicker noise. Second, IF digitization allows quadrature mixing to be realized in the digital domain with low power consumption, perfect linearity and matching for excellent image rejection performance. However, as the sampling frequency of ADC is at least twice the IF, the ADC may be much less power efficient, especially for traditional Nyquist-rate ADC in high IF application. Furthermore, the IF channel selection filter can be shifted to digital domain. A wideband ADC digitizes all channels and channel selection can be done in the DSP, as shown in Figure 1.1(b). The wideband IF digitization receiver is especially advantageous in a base station, where only one receiver board is required to process all channels. In this case, a high power consumption brought by the wideband ADC can be tolerated. However, the lack of analog channel filtering puts harsh requirement on the linearity and dynamic range of the ADC.

1.1 Bandpass ΣΔ ADC for IF Digitization

The candidate for the ADC in IF digitization receiver can be either wideband Nyquist-rate ADC or bandpass sigma-delta (ΣΔ) ADC. The latter is the optimum solution since the bandwidth of IF signal is typically much smaller than the carrier frequency, and hence, reducing the quantization noise in the entire Nyquist band becomes inefficient. Instead, by using bandpass ΣΔ ADC the quantization noise power is reduced only in a narrowband around the IF, thus yielding high resolution at IF and relatively low power consumption [6]. In general, a bandpass ΣΔ ADC is composed of a bandpass sigma-delta modulator (ΣΔM) and a digital decimation filter. Bandpass ΣΔMs can be realized in both discrete- and continuous-time (DT and CT) domains. The former refers to the ΣΔMs implemented using switch-capacitor (SC) loop filters, while the latter is realized using active-RC, transconductor-C (G_m-C) or LC filter.

DT bandpass ΣΔMs are able to achieve robust performance, but only at low speed. In most receivers where DT bandpass ΣΔM is employed, the RF signal has to be down-converted to a low IF around 10-20MHz before it is digitized [7-12]. Although high frequency DT bandpass ΣΔMs around 100MHz have been reported, signal has to be translated to a low IF through sub-sampling before it can be digitized [13-15]. Attempts have been made to push the IF to a higher frequency, but so far the highest center frequency of the DT bandpass ΣΔMs that have been reported is 60MHz [16]. In addition, double-sampled SC loop filter has been used to bring down the clock frequency while maintaining the high center frequency [16-21]. The major bottleneck for the high speed DT ΣΔMs is the settling time of the SC filter, which requires the opamp to have very large bandwidth. CT bandpass ΣΔMs with center frequency from sub-hundred-megahertz to gigahertz have been reported [22-35]. Most of them (above 100MHz) were realized in SiGe or III-V processes. In general, the performance of CT bandpass ΣΔMs

cannot match those of DT ones in terms of dynamic range and SNR. There are a number of reasons. Some of them are inherent in CT ΣΔMs, such as excess loop delay and clock jitter noise. In narrowband digitization, the non-idealities of constituent active-RC, Gm-C and LC resonators are also the limiting factors. Firstly, it is difficult to realize the resonator or bandpass loop filter with high Q factor due to the parasitic loss, especially at high frequencies. Although Q enhancement circuit can be employed, the linearity of the resonator will be deteriorated [25]. Secondly, the resonant frequency of the resonator is subject to the process variation and temperature. Automatic tuning circuit is normally required. However, it still proves difficult to achieve high accuracy, especially in the case of narrowband digitization. The resultant shift of the center frequency greatly degrades the performance of the bandpass ΣΔM.

1.2 Motivation and Scope

It is well known that electromechanical resonators, such as surface acoustic wave (SAW) and micro-mechanical (MEMS) resonator, possess very high Q factor (typically unloaded Q from 1000-10000). In addition, they offer accurate resonant frequency and wide resonant frequency range. This opens the possibility of using electromechanical resonator to replace its electronic counterpart and realize high-performance bandpass ΣΔMs. Moreover, the advent of micromachining technology allows some types of electromechanical resonators to be realized on silicon substrate. Thus, the integration of electromechanical resonator and electronic circuits is possible. High-Q electro-mechanical resonators based ΣΔMs are suitable for narrowband digitization. For wideband applications, electromechanical filter may be used, since its bandwidth can be customized according to the applications.

The scope of this thesis is to investigate the feasibilities of electromechanical resonators/filters based bandpass ΣΔMs and understand the issues in realizing such bandpass ΣΔMs with SAW and MEMS resonators/filters. Due to the limitations of available fabrication technologies, the fully monolithic implementation is not attempted. The thesis mainly focuses on the bandpass ΣΔMs with externally connected electromechanical resonators/filters. Although off-chip resonators/filters may be a disadvantage, hybrid realization is possible and acceptable if it can be justified by its performance.

1.3 Organization of the Thesis

The thesis is organized as follows. Chapter 2 reviews the concept of bandpass ΣΔMs and conventional bandpass ΣΔMs. Chapter 3 describes architectures and the system-level design of the electromechanical resonator based bandpass ΣΔM. Chapter 4 focuses on the design of the electromechanical filter based bandpass ΣΔM. Chapter 5 gives the circuit-level implementation of the electromechanical resonators based bandpass ΣΔMs and the experimental results. Chapter 6 presents a prototype of the 4^{th}-order bandpass ΣΔM employing only one SAW filter and measurement results. Chapter 7 gives conclusions and recommendations for future work.

CHAPTER 2

BANDPASS SIGMA-DELTA MODULATORS

In this chapter, a review of bandpass ΣΔMs is presented. It starts from a brief introduction of the ΣΔ modulation followed by a review of previously published bandpass ΣΔMs. Limitations of DT and CT resonators in conventional bandpass ΣΔMs are also discussed and the motivation of replacing them with electromechanical resonators is briefly described.

2.1 Fundamentals of Sigma-Delta Modulators

2.1.1 Nyquist Rate ADCs

Analog-to-digital conversion is traditionally described in terms of two separated operation: uniform sampling in time and quantization in amplitude. According to the Nyquist theorem, the sampling frequency f_s should be at least two times larger than input signal bandwidth f_B for error-free reconstruction of the input signal [36], which is given by

$$f_s \geq 2f_B \tag{2.1}$$

The sampling frequency, which is two times of the signal bandwidth, is called Nyquist sampling rate. In real application, to alleviate the constraints on anti-aliasing filters, sampling frequency is sometimes chosen to be slightly higher than the Nyquist sampling rate. Such ADCs are called Nyquist-rate ADCs, as shown in Figure 2.1.

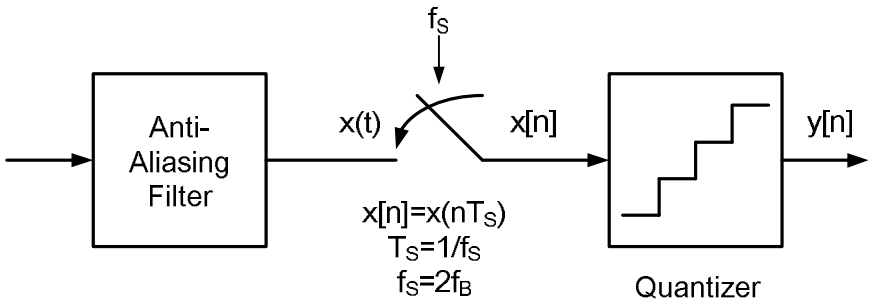


Figure 2.1 Nyquist-rate ADC

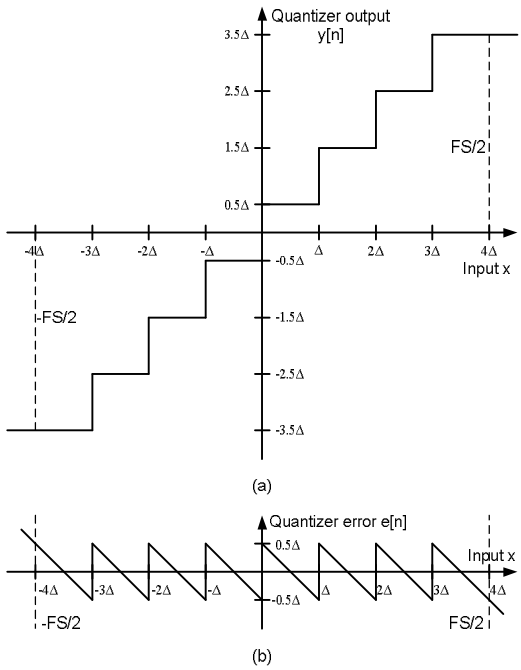


Figure 2.2 Transfer characteristic and error characteristic of 3 bit uniform quantizer

The sampled signal is quantized in amplitude to a finite set of output values. The typical transfer characteristic and error characteristic of a three bit uniform quantizer are shown in Figure 2.2. The quantization is a non-invertible process and there is inherent quantization error because a continuous range of amplitude is mapped into a finite set of digital output code. A unity gain, uniform N-bit quantizer has 2^N quantization levels, and the step size between quantization levels is

$$\Delta = \frac{FS}{2^N - 1} \approx \frac{FS}{2^N} \tag{2.2}$$

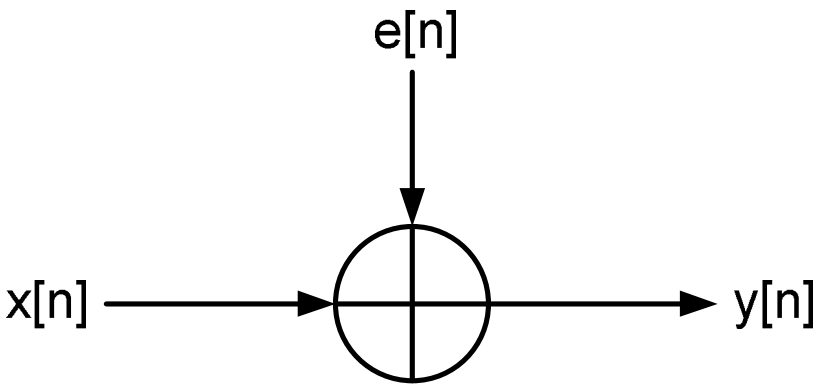


Figure 2.3 Linearized, stochastic model of quantizer

where FS is the full scale input range of the quantizer. The approximation in (2.2) can be made if N is large. The quantizer, which is a non-linear system, is difficult to analyze. But it can be approximated with a linear model and is shown in Figure 2.3.

In this model, the non-linear quantization error is approximated as an additive white noise $e[n]$ which is uniformly distributed over $[-\Delta/2, \Delta/2]$ with zero mean, and then the quantizer can be analyzed using statistical methods [37] and modeled as

$$y[n] = x[n] + e[n] \tag{2.3}$$

This approximation is nevertheless useful to predict the performance of ADC, even though there exist some limitations. Under these assumptions, the variance σ_e^2 of the quantization error (noise) $e[n]$, i.e, power P_n of the quantization noise can be expressed as

$$P_n = \sigma_e^2 = \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} e^2 de = \frac{\Delta^2}{12} \tag{2.4}$$

Assuming that the largest sinusoidal input (full scale input) which does not overload the ADC has an amplitude of FS, then the peak signal-to-noise ratio ($SNR_{\max}$) is given by

$$SNR_{\max} = 10\log\left(\frac{FS^2}{8} / P_n\right) \cong 6.02N + 1.76\ (dB) \tag{2.5}$$

This is also the dynamic range (DR) value for Nyquist rate ADC. An increase in resolution can be obtained by increasing the number of quantizer's bits, a method not always convenient since the complexity of the ADC is exponentially increasing with the number of bits. Furthermore, if the signal is sampled too close to the Nyquist rate, the anti-aliasing filter must have a very sharp cutoff, which is non-trivial for the design of the analog filters.

2.1.2 Oversampled ADCs

Benefiting from today's advanced VLSI technology, it is possible to sample the input analog signal at a rate much higher than the Nyquist rate, which results in an oversampled ADC, as shown in Figure 2.4. The oversampling ratio (OSR) is defined as

$$OSR = \frac{f_s}{2f_B} \tag{2.6}$$

The oversampled ADC with N bits quantizer adds the same quantization noise power to the quantized signal as a Nyquist rate ADC with N bits does. The difference is that only part of the quantization noise power falls in the signal bandwidth since the equivalent bandwidth of the quantization noise spans from DC to $f_s/2$. Figure 2.5 shows the power spectral densities (PSDs) for both Nyquist rate and oversampled ADCs. The in-band noise power of the oversampled ADC , P_{nib}, is given by

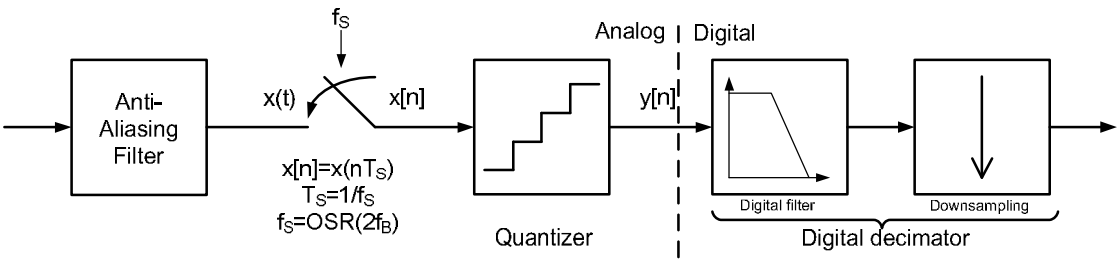


Figure 2.4 Oversampled ADC

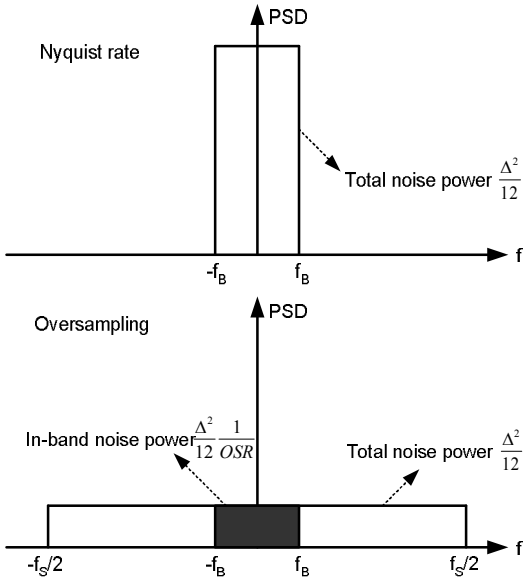


Figure 2.5 Quantization noise PSDs of Nyquist rate and oversampled ADCs

$$P_{nib} = \int_{-f_B}^{f_B} \frac{\sigma_e^2}{f_s} df = \sigma_e^2 \frac{2f_B}{f_s} = \frac{\Delta^2}{12}\frac{1}{OSR} \tag{2.7}$$

The $SNR_{\max}$ is

$$SNR_{\max} = 10\log\left(\frac{FS^2}{8} / P_{nib}\right) \cong 6.02N + 1.76 + 10\log OSR\ (dB) \tag{2.8}$$

The $SNR_{\max}$ is improved by about 3dB, which is equivalent to 0.5bit, for every doubling of the OSR.

Oversampling improves the SNR, but only by a limited amount. To further increase the in-band SNR, a technique named noise-shaping is used to reduce the in-band noise, which result in the sigma-delta (ΣΔ) ADC.

2.1.3 ΣΔ ADCs

Figure 2.6 shows a typical ΣΔ ADC, which is composed of an anti-aliasing filter, a sample-and-hold circuit, a sigma-delta modulator (ΣΔM) and a digital decimator [38][39]. The core of the ΣΔ ADC is the ΣΔM, as shown in the dash-line box.

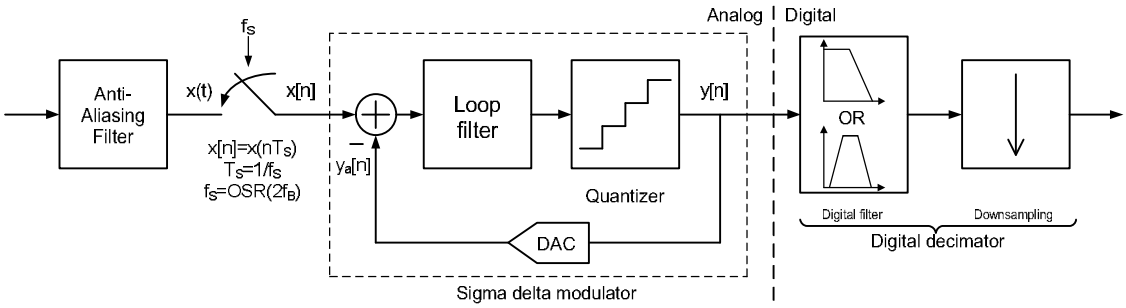


Figure 2.6 ΣΔ ADC

The ΣΔM consists of a loop filter (lowpass or bandpass), an internal coarse ADC or quantizer, and a digital-to-analog converter (DAC) in the feedback path. The noise shaping is performed by the loop filter in the forward path of the ΣΔM. The loop filter can be either discrete or continuous-time filter. The ΣΔM can be analyzed using linear model with a linearized quantizer. Figure 2.7 shows the linear model of the discrete-time (DT) ΣΔM, where the quantization noise is modeled as an additive white noise, *H(z)* is the transfer function of loop filter in DT domain and an ideal DAC in the feedback path is assumed. The output of this linear model can be expressed as

$$Y(z) = \frac{H(z)}{1+H(z)} X(z) + \frac{1}{1+H(z)} E(z) \tag{2.9}$$

This equation (2.9) shows that the input signal and the quantization noise are modified by different transfer functions, as given below

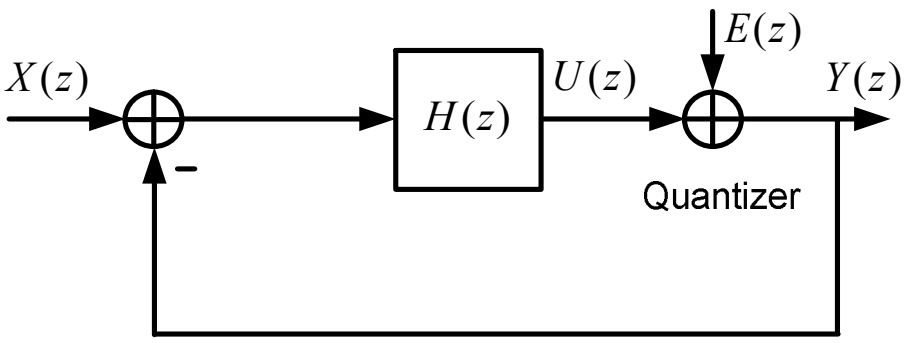


Figure 2.7 Linear model of DT ΣΔM

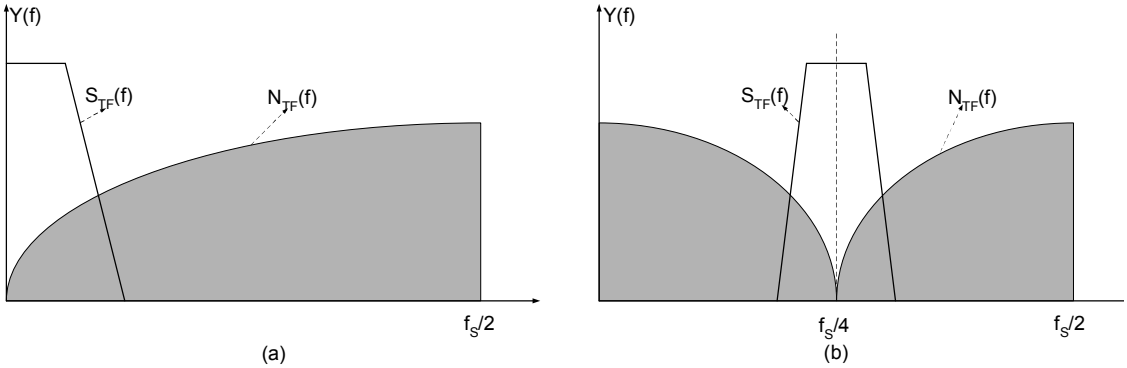


Figure 2.8 Illustration of noise shaping concept in (a) lowpass and (b) bandpass ΣΔMs

$$S_{TF}(z) = \frac{H(z)}{1+H(z)}$$
$$N_{TF}(z) = \frac{1}{1+H(z)} \tag{2.10}$$

where $S_{TF}(z)$ denotes the signal transfer function (STF) and $N_{TF}(z)$ is the noise transfer function (NTF). By properly choosing the loop filter transfer function $H(z)$, the in-band quantization noise can be greatly suppressed. This concept is illustrated in Figure 2.8 for both lowpass and bandpass noise shaping.

2.1.4 Examples of DT Lowpass ΣΔMs

The block diagram of the 1st-order DT lowpass ΣΔM is shown in Figure 2.9, where the loop filter $H(z) = z^{-1}/(1-z^{-1})$ is simply an integrator with a pole at DC. Using linear model, the transfer function is given by

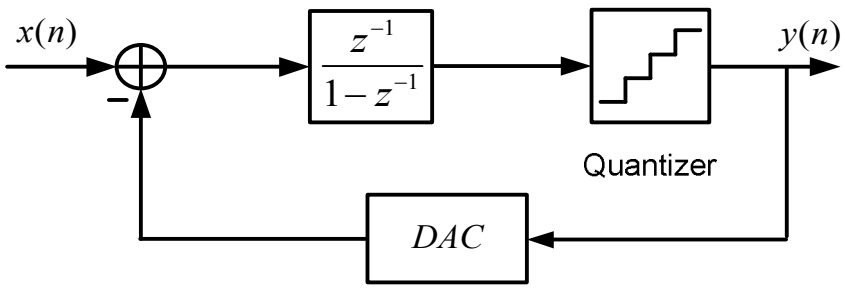


Figure 2.9 1st-order DT lowpass ΣΔM

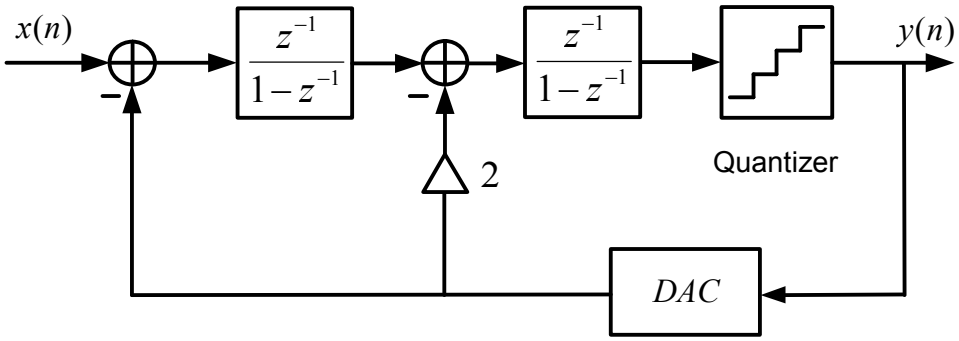


Figure 2.10 2nd-order DT lowpass ΣΔM

$$Y(z) = X(z)z^{-1} + E(z)(1-z^{-1}) \tag{2.11}$$

From (2.11) the STF and the NTF are

$$S_{TF}(z) = z^{-1} \quad and \quad N_{TF}(z) = 1 - z^{-1} \tag{2.12}$$

Clearly, the STF leaves the signal unaltered, just delayed by one clock cycle, whereas the NTF (1st-order differentiator) high-passes the quantization noise. Similarly, a 2nd-order ΣΔM can be constructed, as shown in Figure 2.10. Its transfer function is

$$Y(z) = X(z)z^{-2} + E(z)(1-z^{-1})^2 \tag{2.13}$$

More in-band quantization noise suppression is provided by 2nd-order high-pass noise shaping. A typical simulated output spectrum of the 2nd-order lowpass ΣΔM is illustrated

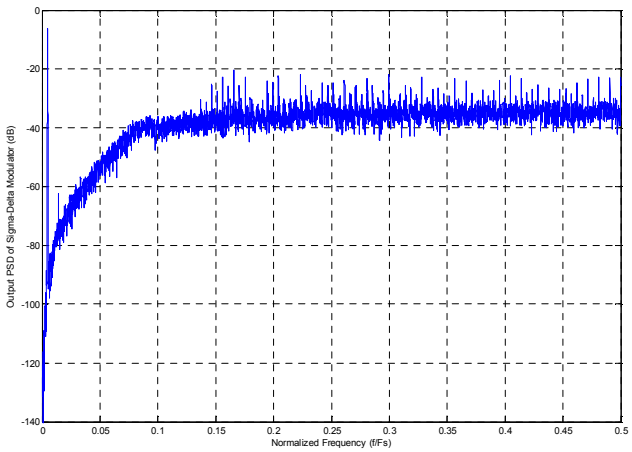


Figure 2.11 Typical output spectrum of a 2nd-order lowpass ΣΔM

in Figure 2.11.

More efficient quantization noise suppression can be achieved by further increasing the order of the loop filter. For the lowpass DT ΣΔM with NTF $N_{TF}(z)=(1-z^{-1})^{L}$, where L is the order of the loop filter, the in-band noise can be calculated as

$$\begin{aligned} P_{nib} &= \int_{-f_B}^{f_B} \frac{\sigma_e^2}{f_s} \left|1-z^{-1}\right|^{2L} df = \int_{-f_B}^{f_B} \frac{\sigma_e^2}{f_s} \left|2\sin(\frac{\pi f}{f_s})\right|^{2L} df \\ &\approx \sigma_e^2 \frac{\pi^{2L}}{2L+1}\left(\frac{2f_B}{f_s}\right)^{2L+1} = \frac{\Delta^2}{12}\frac{\pi^{2L}}{2L+1}\frac{1}{OSR^{2L+1}} \end{aligned} \tag{2.14}$$

Thus the peak SNR obtained is

$$SNR_{\max} \cong 6.02N + 1.76 + (2L+1)10\log(OSR) - 10\log\left(\frac{\pi^{2L}}{2L+1}\right)(dB) \quad N>3 \tag{2.15}$$

If single-bit quantizer (N=1) is used, the peak SNR becomes

$$SNR_{\max} = 1.76 + (2L+1)10\log(OSR) - 10\log\left(\frac{\pi^{2L}}{2L+1}\right)(dB) \quad N=1 \tag{2.16}$$

The $SNR_{\max}$ improves by $3(2L+1)$ dB, which is equivalent to $(L+0.5)$ bit, for every doubling of OSR.

2.1.5 Examples of DT Bandpass ΣΔMs

Bandpass ΣΔM differs from the lowpass one only in its loop filer. For the bandpass ΣΔM, the loop filter is also bandpass, which has maximum gain in the passband, and hence suppresses the in-band quantization noise since the signal band is centered at the center frequency of the loop filter. The OSR for the bandpass ΣΔM is defined as

$$OSR = \frac{f_s}{2f_B} \tag{2.17}$$

Note that the OSR is the ratio of sampling frequency f_s to twice of the signal bandwidth f_B, not the center frequency f_c. A common consideration is to place the center frequency

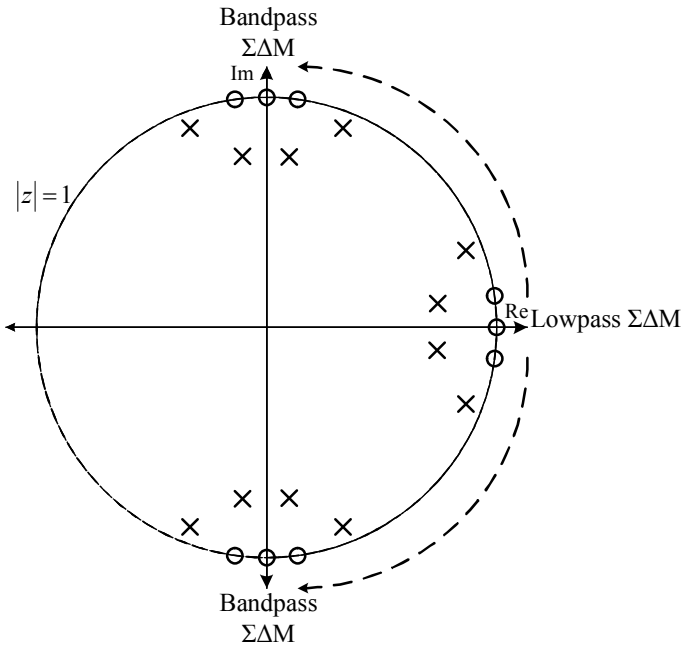


Figure 2.12 Lowpass-to-bandpass transformation

at frequencies which are simple fraction of f_s, such as $f_s/4$ and $f_s/2$, which facilitates both circuit and decimation algorithm design [38].

Since lowpass ΣΔMs and their properties are well-studied, the simplest way to design the NTF for a DT bandpass ΣΔM is to start with a suitable lowpass modulator and apply lowpass-to-bandpass transformation [38], which is given by

$$z \to -z^2 \tag{2.18}$$

The transformation maps zeros of the NTF of lowpass ΣΔMs from DC ($z=1$) to one quarter of the sampling frequency $f_s/4$ ($z=\pm j$) . This transformation is illustrated in Figure 2.12. In practice, this transformation means to replace the integrator in lowpass ΣΔMs by a resonator whose center frequency is at $f_s/4$, as given below

$$\frac{z^{-1}}{1-z^{-1}} \xrightarrow{z\to -z^2} \frac{-z^{-2}}{1+z^{-2}} \tag{2.19}$$

The *L-th* order high pass NTF is transformed to *2L-th* order band-rejected (notch) NTF

$$(1-z^{-1})^L \xrightarrow{z\to -z^{-2}} (1+z^2)^L \tag{2.20}$$

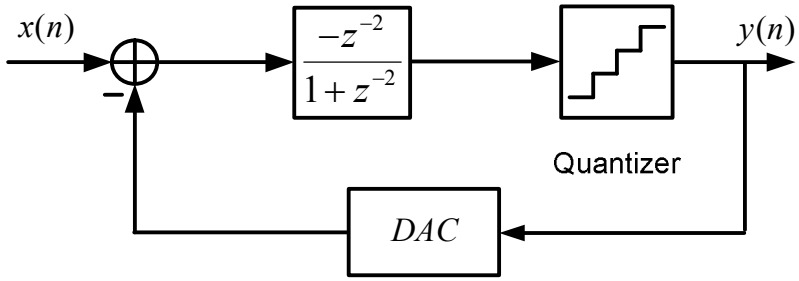


Figure 2.13 2nd-order DT bandpass ΣΔM

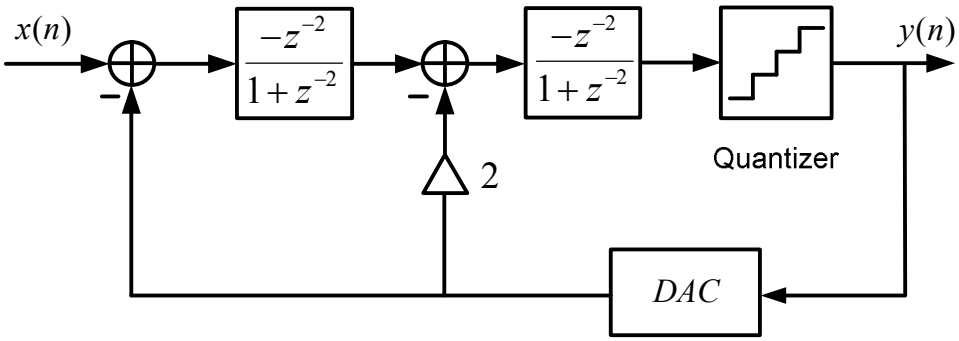


Figure 2.14 4th-order DT bandpass ΣΔM

The resultant 2nd- and 4th- order bandpass ΣΔMs, which are corresponding to the lowpass ΣΔMs given in Figure 2.9 and Figure 2.10, are shown in Figure 2.13 and 2.14, respectively. The simulated output spectrum of the 4th-order bandpass ΣΔM is given in Figure 2.15. The advantage of this transformation is that the properties of the lowpass prototype, such as stability and noise performance, are preserved. In addition, signal band is center at $f_s/4$, allowing for simple decimator design. A more general lowpass to bandpass transformation is

$$z \to -z\frac{z+a}{az+1}, \quad -1 < a < 1 \tag{2.21}$$

and it enables full control of the notch frequency through the parameter *a*. However, the dynamic properties of the lowpass prototype are not preserved [38]. The lowpass to bandpass transformation doubles the order of the loop filter and hence, in principle, doubles the number of required active components.

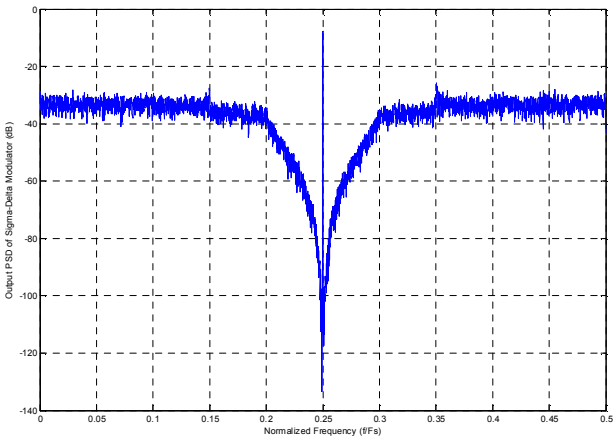


Figure 2.15 Typical output spectrum of a 4[th]-order bandpass ΣΔM

A similar calculation of the in-band quantization noise in the DT bandpass ΣΔM with $N_{TF}(z)=(1+z^{-2})^L$ is given by

$$\begin{aligned} P_{nib} &= \left(\int_{-\frac{f_s}{4}-\frac{f_B}{2}}^{-\frac{f_s}{4}+\frac{f_B}{2}} + \int_{\frac{f_s}{4}-\frac{f_B}{2}}^{\frac{f_s}{4}+\frac{f_B}{2}}\right)\frac{\sigma_e^2}{f_s}\left|1+z^{-2}\right|^{2L} df \\ &= \int_{\frac{f_s}{4}-\frac{f_B}{2}}^{\frac{f_s}{4}+\frac{f_B}{2}} \frac{2\sigma_e^2}{f_s}\left|2\cos(\frac{2\pi f}{f_s})\right|^{2L} df = \int_{\frac{f_s}{4}-\frac{f_B}{2}}^{\frac{f_s}{4}+\frac{f_B}{2}} \frac{2\sigma_e^2}{f_s}\left(4\sin^2(\frac{\pi}{2}-\frac{2\pi f}{f_s})\right)^L df \\ &\cong \int_{\frac{f_s}{4}-\frac{f_B}{2}}^{\frac{f_s}{4}+\frac{f_B}{2}} \frac{2\sigma_e^2}{f_s} 2^{2L}(\frac{\pi}{2}-\frac{2\pi f}{f_s})^{2L} df = \frac{\Delta^2}{12}\frac{\pi^L}{2L+1}\frac{1}{OSR^{2L+1}} \end{aligned} \tag{2.22}$$

which is the same as the in-band quantization noise of the lowpass DT ΣΔM given in (2.14). This is not a surprising result.

2.1.6 Stability Considerations

Although the quantization noise can be suppressed more effectively through the use of high-order loop filter, the order of the bandpass ΣΔM with $N_{TF}(z)=(1+z^{-2})^L$ cannot be increased arbitrarily because it is difficult to guarantee the stability when the order is six or higher for single-loop modulators [38]. The stability of the ΣΔM can be qualitatively explained as follows. According to Figure 2.7 and equation (2.9), the input to the quantizer is given by

$$\begin{aligned} U(z) &= Y(z) - E(z) \\ &= S_{TF}(z)X(z) + [N_{TF}(z) - 1]E(z) \end{aligned} \tag{2.23}$$

Assuming that the NTF is in the form $N_{TF}(z) = (1+z^{-2})^L$ (all of its zeros are at $f_s/4$), it has a peak gain of $|N_{TF}(1)| = 2^L$, which leads to a large gain of $[N_{TF}(z) - 1]$ for large L. Consequently, the amplitude of the signal at the input of quantizer can not be well bounded for large L because of the large amplification of out-of-band quantization noise. In this case, the amplitude of the internal signal of the ΣΔM increases rapidly and oscillations may take place. To improve the stability of the high-order single-loop ΣΔM, the loop filter, thus the NTF should be carefully designed with the aid of computer simulation. Generally, the high-order NTF will differ from pure high order notch $(1+z^{-2})^L$.

In order to characterize the stability behavior of non-linear ΣΔM, several methods have been applied, such as describing function method [40-43], positively invariant sets methods [44] and Tsypkin's method [45]. Among them, the describing function method is of great interest. In this method, the nonlinear single-bit quantizer is modeled by a quasi-linear, signal dependent gain stage together with a phase shift [43]. After this quasi-linearization, root locus method can be used to analyze the stability of ΣΔM by varying the signal dependent gain.

In addition to the analytical methods, several stability criteria have been introduced for the practical design of stable high-order ΣΔMs and have been adopted extensively by designers. Most of them try to design a NTF with well bounded magnitude, as discussed at the beginning of this section. The most widely-used criterion is the Lee's criterion [46][47] and its modified version [48], that is

A ΣΔM with $NTF = N_{TF}(z)$ is tended to be stable if $\max|N_{TF}(e^{j\omega})| < 2$ or 1.5.

Note that this criterion is neither necessary nor sufficient to guarantee stability and needed to be verified by extensive simulations for any specific higher-order design.

2.1.7 Continuous-Time Vs. Discrete-Time

Until now, the loop filters of the ΣΔMs are considered to be discrete-time (*z* domain). Although it simplifies the understanding of the noise shaping concepts and corresponds directly to a switch-capacitor implementation, it is not the only form of implementation. The loop filter can also be realized in the continuous-time (CT) domain [49]. A typical structure of the CT ΣΔM is shown in Figure 2.16. In CT ΣΔM, the sampling of the signal occurs after the loop filter and is at the input of the quantizer, instead of at the input of the modulator as in the DT ΣΔM. In practice, the sampling circuit can be combined with the quantizer [50]. Similar to the DT ΣΔM, the quantized output of the CT ΣΔM is fed back to the input through DAC. However, in CT ΣΔM, the type of the DAC and its output waveforms play a significant role on the overall performance of the ΣΔM. A generalized output waveform of three commonly used rectangle DACs can be illustrated in Figure 2.17. They are non-return-to-zero (NRZ, $t_1 = 0$ and $t_2 = T_s$), return-to-zero (RZ, $t_1 = 0$ and $t_2 = T_s / 2$) and half-delay-return-to-zero (HRZ, $t_1 = T_s / 2$ and $t_2 = T_s$) [51].

Compared with the DT ΣΔM, CT realization has the following potential advantages.

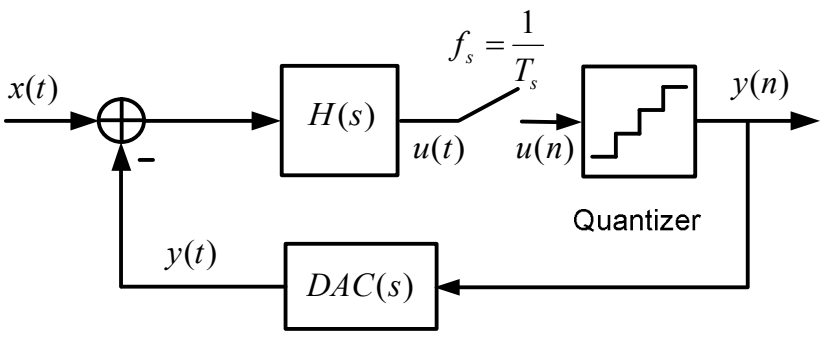


Figure 2.16 CT ΣΔM

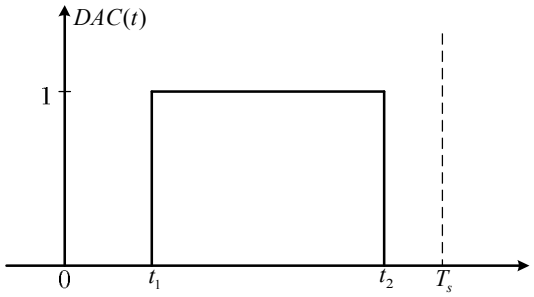


Figure 2.17 Rectangle DAC output waveform

- **High speed.** Unlike the DT ΣΔM (implemented by switched-capacitor circuits), which requires the opamp to have wide bandwidth (usually at least five times the sampling frequency [52]) to reduce the settling error, the CT ΣΔM samples the signal at the input of the quantizer and therefore the sampling error is suppressed by the noise shaping mechanism. Besides, no settling is involved in CT loop filters. Thus, CT ΣΔMs can potentially operate at high sampling frequencies [51].
- **Inherent anti-aliasing filtering**. As mentioned before, the quantization in the CT ΣΔM occurs inside the feedback loop, at the input of the quantizer. The CT loop filter provides an inherent anti-aliasing function so that anti-aliasing filter that precedes the ΣΔM is no longer needed, or much relaxed and easy to be implemented [50].
- **Low supply voltage operation.** As the supply voltage scaled down in deep sub-micron CMOS process, it becomes even more difficult to realize MOS switches with high linearity and low on-resistance. DT ΣΔM, which requires switches, has to use extra circuit techniques to overcome this problem, such as switch-bootstrapping [53-56] and switched-opamp (SO) [21][57-61]. However, CT ΣΔM does not have this problem and hence it is suitable for low voltage operation.

- **Low power consumption.** The opamps in CT ΣΔMs do not have settling problems; their bandwidth requirement can be much relaxed. Therefore, for the same signal bandwidth and resolution requirements, CT ΣΔMs need much less power than DT ΣΔMs do, especially for wideband conversion.

CT ΣΔM, however, has its own weaknesses. It is more sensitive to clock jitter which introduces the error in the feedback DAC. It is also subject to process and temperature variation (PTV). In general, the CT loop filter coefficients and frequency response are determined by the absolute values of onchip resistance, capacitance, inductance and transconductance, depending on the types of the filter used. Unfortunately, all these values are subject to the PTV and tuning is therefore needed for practical CT ΣΔMs.

2.1.8 Equivalence between DT ΣΔMs and CT ΣΔMs

The overall behavior of a CT ΣΔM loop is nonetheless discrete time due to the fact that the loop is sampled in time domain by the clocked quantizer. Thus, design and simulation of the ideal CT ΣΔM can be done in discrete-time domain. Subsequently, the originated DT open loop filter function $H(z)$ can be replaced by a CT equivalent $H(s)$ according to impulse-invariant transformation [50][51], as shown in Figure 2.18. It requires that, at the sampling instant, both CT and DT modulators depicted in Figure 2.18 produce the same output $u(n)$ at the input of quantizer for the same $y(n)$, that is

$$u(n) = u(t)\big|_{t=nT_s} \tag{2.24}$$

This leads to the condition

$$Z^{-1}\{DAC_D(z)H(z)\} = L^{-1}\{DAC_C(s)H(s)\}\big|_{t=nT_s} \tag{2.25}$$

where $DAC_D(z)$ and $DAC_C(s)$ denote the transfer functions of DACs in DT ΣΔM and CT ΣΔM respectively. Generally, $DAC_D(z) = 1$, we have

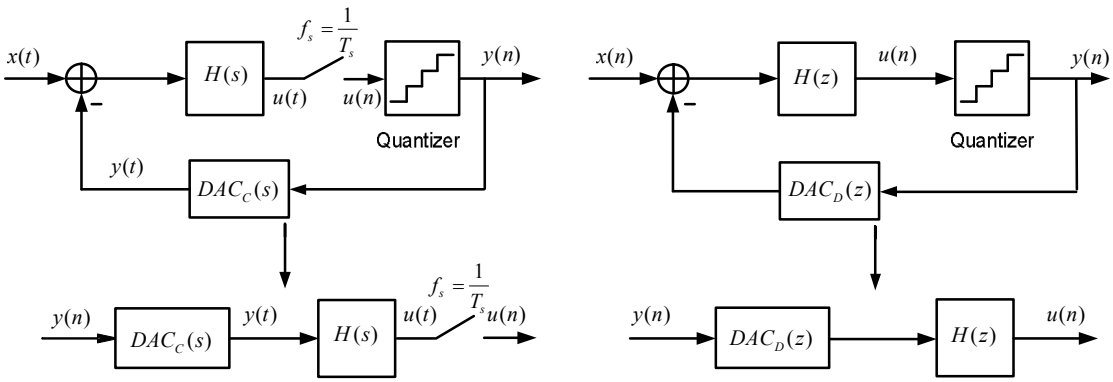


Figure 2.18 Equivalence between CT and DT ΣΔM

$$Z^{-1}\{H(z)\} = L^{-1}\{DAC_C(s)H(s)\}\Big|_{t=nT_s} \tag{2.26}$$

or in the time domain

$$h(n) = \left[dac_C(t) * h(t)\right]\Big|_{t=nT_s} = \int_{-\infty}^{\infty} dac_C(\tau)h(t-\tau)d\tau\Big|_{t=nT_s} \tag{2.27}$$

Thus CT loop filter $H(s)$ can be built by first choosing a DAC output waveform $dac_C(t)$, then using (2.26) or (2.27) to find $H(s)$. As shown in Figure 2.17, the output of the DAC can be expressed in time domain as

$$dac(t) = \begin{cases} 1, & 0 \le t_1 < t < t_2 \le T_s \\ 0, & otherwise \end{cases} \tag{2.28}$$

where a rectangular DAC output waveform of magnitude 1 is assumed, The Laplace transform of (2.28) is

$$DAC_C(s) = \frac{e^{-t_1 s} - e^{-t_2 s}}{s} \tag{2.29}$$

To find $H(s)$, $H(z)$ is expressed as a partial fraction expansion. Each term can be then converted from *z* domain to *s* domain using the table given in [51]. The combination of partial fractions in *s* domain will be the equivalent CT transfer function $H(s)$. For example, given the loop filter transfer function of a 2nd-order lowpass DT ΣΔM

$$H(z)=\frac{-2z+1}{(z-1)^2} \tag{2.30}$$

with NRZ DAC $(t_1,t_2)=(0,T_s)$, the equivalent CT loop filter is

$$H(s)=-\frac{1+1.5s}{s^2} \tag{2.31}$$

In the case of RZ DAC $(t_1,t_2)=(0,0.5T_s)$, the CT loop filter transfer function becomes

$$H(s)=-\frac{2+2.5s}{s^2} \tag{2.32}$$

A method suitable for automatic transforming between DT and CT ΣΔMs using computer program is realized by applying the concept of state space [38]. Figure 2.19 illustrates this mapping. Without loss of generality, the sampling period $T_s=1\text{sec}$ is assumed. The state equations for the linear parts of CT and DT ΣΔMs presented in Figure 2.19 are, respectively,

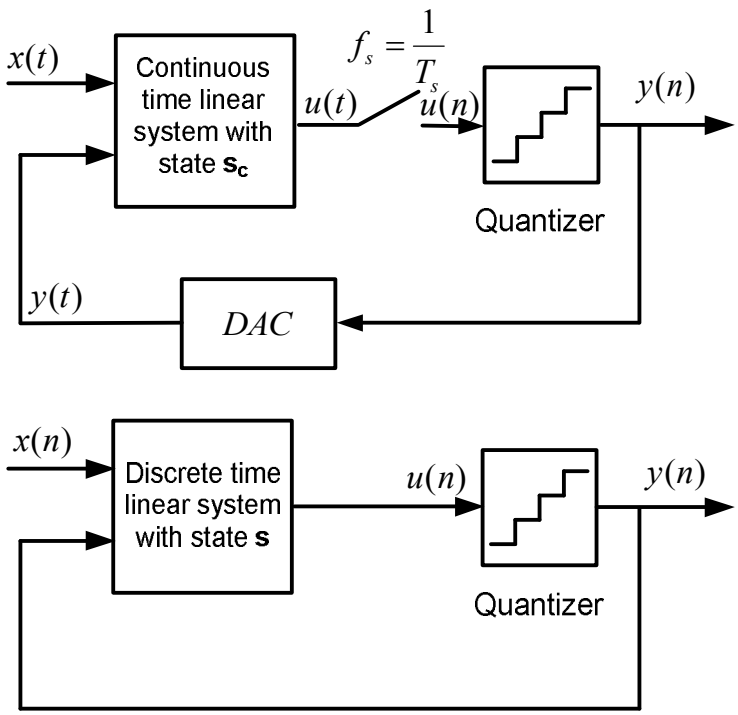


Figure 2.19 Equivalence between CT ΣΔM and DT ΣΔM using state space concept

$$\dot{s}_c(t) = \boldsymbol{A}_c s_c(t) + \boldsymbol{B}_c \begin{bmatrix} x(t) \\ y(t) \end{bmatrix} \tag{2.33}$$

and

$$s(n+1) = \boldsymbol{A} s(n) + \boldsymbol{B} \begin{bmatrix} x(n) \\ y(n) \end{bmatrix} \tag{2.34}$$

$\boldsymbol{A}_c$ and $\boldsymbol{A}$ are matrices describing the interconnections between the states. $\boldsymbol{B}_c$ and $\boldsymbol{B}$ are $n \times 2$ matrices which describe the feed-ins for each input. Equation (2.33) can be solved to yield following equation,

$$s_c(t) = e^{\boldsymbol{A}_c t} s_c(0) + e^{\boldsymbol{A}_c t} \int_0^t e^{-\boldsymbol{A}_c \tau} \boldsymbol{B}_c \begin{bmatrix} x(\tau) \\ y(\tau) \end{bmatrix} d\tau \tag{2.35}$$

The sample of $s_c(t)$ at nT_s can be obtained with rectangle DAC waveform given in Figure 2.17 assumed, that is

$$s_c(n+1) = e^{\boldsymbol{A}_c} s_c(n) + \int_{1-t_2}^{1-t_1} e^{\boldsymbol{A}_c \tau} \boldsymbol{B}_{c1} x(n+1-\tau) d\tau + \int_{1-t_2}^{1-t_1} e^{\boldsymbol{A}_c \tau} \boldsymbol{B}_{c2} y(n+1-\tau) d\tau \tag{2.36}$$

where $\boldsymbol{B}_c = \begin{bmatrix} \boldsymbol{B}_{c1} & \boldsymbol{B}_{c2} \end{bmatrix}$, The first integral in (2.36) can be ignored [49] and thus (2.36) becomes

$$s_c(n+1) = e^{\boldsymbol{A}_c} s_c(n) + \boldsymbol{A}_c^{-1} \left(e^{\boldsymbol{A}_c (1-t_1)} - e^{\boldsymbol{A}_c (1-t_2)} \right) \boldsymbol{B}_{c2} y(n) \tag{2.37}$$

In order for the CT and DT systems to be equivalent, the following conditions need to be satisfied

$$\boldsymbol{A} = e^{\boldsymbol{A}_c} \quad \text{and} \quad \boldsymbol{B}_2 = \boldsymbol{A}_c^{-1} \left(e^{\boldsymbol{A}_c (1-t_1)} - e^{\boldsymbol{A}_c (1-t_2)} \right) \boldsymbol{B}_{c2} \tag{2.38}$$

where $\boldsymbol{B} = \begin{bmatrix} \boldsymbol{B}_1 & \boldsymbol{B}_2 \end{bmatrix}$. (2.38) converts a CT ΣΔM to its DT equivalence. The inverse transformation

$$\boldsymbol{A}_c = \log \boldsymbol{A} \quad \text{and} \quad \boldsymbol{B}_{c2} = \boldsymbol{A}_c \left(e^{\boldsymbol{A}_c (1-t_1)} - e^{\boldsymbol{A}_c (1-t_2)} \right)^{-1} \boldsymbol{B}_2 \tag{2.39}$$

converts a DT ΣΔM to its CT equivalence. A Matlab program is written to perform the above transformation.

2.1.9 Performance Metrics

Generally, both static and dynamic metrics are used to characterize ADCs. The static metrics, such as offset, gain errors, differential non-linearity (DNL), and integral non-linearity (INL), are mainly used to describe the transfer characteristic or DC performance of Nyquist ADC and therefore will not be explained. The dynamic metrics, as its name implies, are used to measure dynamic or AC performance of the ADC. Commonly used dynamic metrics as measurements of the resolution include *SNR*, dynamic range (*DR*), and effective number of bits (*ENOB*). Those related to the linearity are harmonic distortion (*HDx*), spurious-free dynamic range (*SFDR*), and third-order intermodulation distortion (*IM3*). Sometimes, signal-to-noise-and-distortion (*SNDR*) is also used to take the distortion into account. The definitions of the dynamic metrics are briefly described below.

SNR is ratio of signal power (P_s) over the in-band noise power (P_{nib}). SNR is a function of input signal strength. The SNR reaches maximum at certain input amplitude. If input amplitude is further increased, the SNR may fall due to the increased noise or distortion, as shown in Figure 2.20.

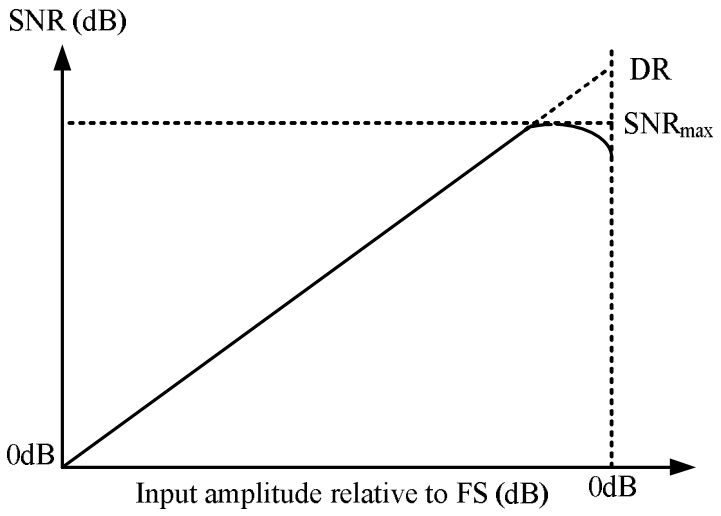


Figure 2.20 Definitions of DR and SNR_{max}

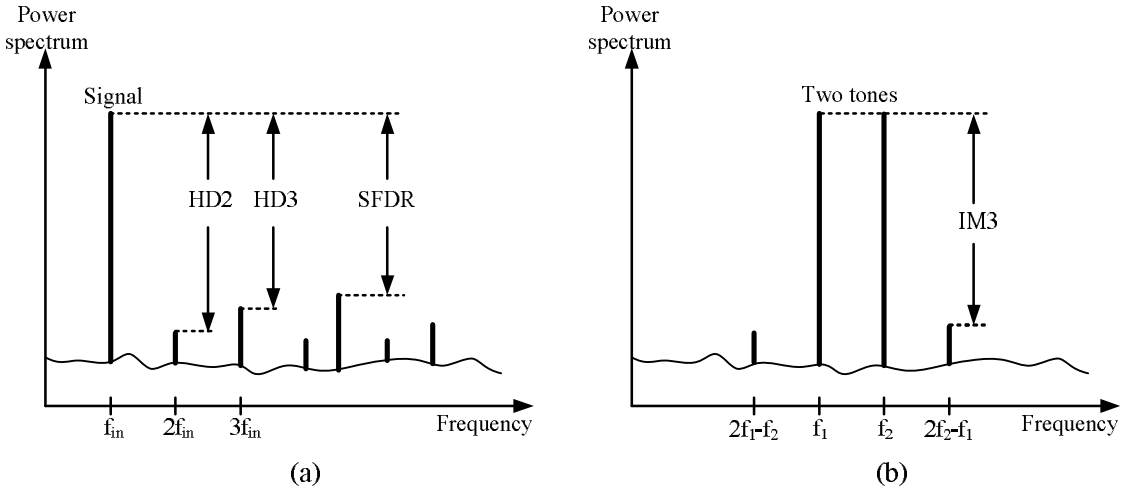


Figure 2.21 Definitions of (a) HD2, HD3, SFDR and (b) IM3

DR is ratio of the maximum signal power (P_{smax}) over the minimum detectable signal power (P_{smin} where *SNR*=0dB) within the signal band, as depicted in Figure 2.20.

$$DR = \frac{P_{smax}}{P_{smin} @ SNR = 0dB} \tag{2.40}$$

HDx is ratio of the signal power over the power of its x^{th} harmonic. *HD2* and *HD3* are most important and shown in Figure 2.21(a).

SFDR is ratio of P_{smax} over the power of the largest in-band spurious tone as indicated in Figure 2.21(a).

IM3 is determined using two input sine waves with frequencies f_1 and f_2. The IM3 is defined as the ratio of the input power over the power of the distortion component at frequency $2f_1$-f_2 or $2f_2$-f_1, as shown in Figure 2.21(b).

SNDR is ratio of the input signal power over the total power of the noise and the distortions (spurious tones) within the band of interest.

ENOB is effective number of bit and defined by

$$ENOB = \frac{SNDR_{max} - 1.76}{6.02} \tag{2.41}$$

which can be used to compare the resolution of ΣΔ ADCs and Nyquist ADCs.

2.2 Review of Bandpass ΣΔMs

Bandpass ΣΔM is seen as a good candidate for IF digitization. After the concept was proposed in 1989 [6], the first monolithic bandpass ΣΔM was reported in 1992 [62]. Since then, many bandpass ΣΔMs, including both DT and CT modulators, have been published for various applications with different IF and bandwidth requirements, such as AM/FM radio, GSM, IS-95 and WCDMA.

In design of the bandpass ΣΔM, the basic design parameters are the loop filter order (L), OSR, and the quantizer resolution (N). Each of them can be increased to improve the resolution of the modulator. First of all, increasing the order of loop filter can improve the SNR quite efficiently. However, as mentioned in section 2.1.6, the single-loop sixth- and higher order bandpass ΣΔMs may be unstable and therefore multi-loop (cascade) architecture is another option to realize higher order bandpass ΣΔMs. Secondly, OSR can be increased until it limits the circuit performance and consume too much power. Furthermore, SNR increases ideally by 6dB with every one bit increase in the resolution of the quantizer. However, the non-linearity of the DAC and the loading of the amplifier in multi-bit bandpass ΣΔMs may limit their performance, especially at high frequency.

In the following sub-sections, the previously published bandpass ΣΔMs will be reviewed, in terms of their architectures, performances and limitations.

2.2.1 DT Single-loop, Single-bit Bandpass ΣΔMs

The DT single-loop, single-bit bandpass ΣΔMs are classified by the orders of their loop filters. Most of the 2nd-order DT bandpass ΣΔMs were published before 2000, and targeted the AM/FM radio application with the signal bandwidth of 9kHz/200kHz centered at 10.7-MHz IF (f_s=42.8MHz) or below [7][58][61][63]. Due to their limited SNDR performance (usually below 50dB in 200-kHz signal bandwidth), these 2nd-order modulators are seldom useful in practical application. A recently published 2nd-order

bandpass ΣΔM achieved a 72-dB SNDR in 200-kHz bandwidth because of its high oversampling ratio (OSR=600). This ΣΔM is sampled at 240MHz using a fast-settling double sampling SC loop filter [16].

4th-order bandpass ΣΔMs are probably the most popular ones because they can provide better performance and are not susceptible to the stability problem [8][9][12][14][15][17][21]. Effective sampling frequency in 4th-order has been pushed up to 160MHz [17] and the narrowband performance has been improved to nearly 80dB in 270-kHz signal band [15]. The wideband performance was also investigated and 48-dB SNDR was achieved in 3.84-MHz bandwidth (WCDMA) [15].

Higher-order single-loop DT bandpass ΣΔMs are difficult to design because of the stability problem. Instead of using lowpass-to-bandpass transformation $z \to -z^2$ as in 2nd- and 4th-order ΣΔMs, the higher-order NTF is synthesized directly through proper placement of its zeros and poles to ensure a stable modulator. A typical structure for a 6th-order bandpass ΣΔM is shown in Figure 2.22 [11]. Efforts have been made to realize 6th- and 8th-order [11][10] modulators, but the performance improvement is not evident. The settling error of the SC resonators seriously compromises the benefit coming from higher-order noise shaping, and may account for the limited performance improvement [11].

Table 2.1 summarizes some typical DT single-loop, single-bit bandpass ΣΔMs. It

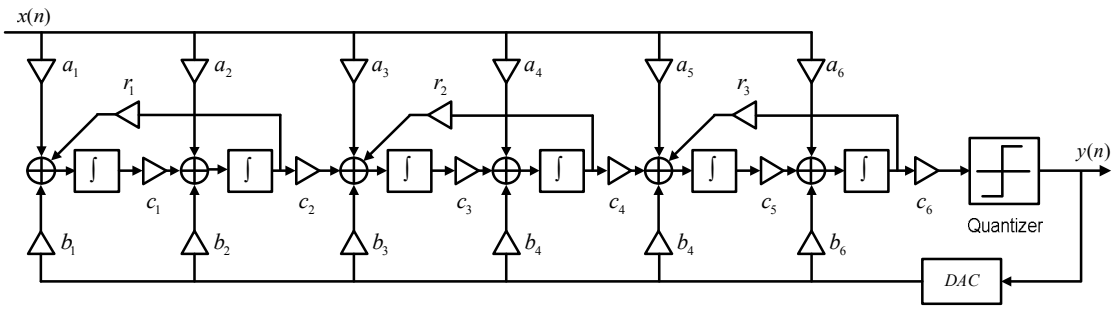


Figure 2.22 A 6th-order bandpass ΣΔM structure proposed in [11]

Table 2.1 Summary of DT single-loop, single-bit bandpass ΣΔMs

Design	[61]	[16]	[14]	[15]	[21]	[11]	[10]
Technology (μm)	0.35/ CMOS	0.35/ CMOS	0.35/ CMOS	0.35/ CMOS	0.25/ CMOS	0.35/ CMOS	0.8/ BiCMOS
Supply Voltage (V)	1	3.3	3	3	1	3.3	±2.5
Type	SO/double sampling	SC/double sampling	SC/sub-ampling	SC/sub-ampling	SO/double sampling	SC	SC
Modulator Order	2	2	4	4	4	6	8
Power (mW)	12	37	56	24	8.45	76	157
Sampling Frequency (MHz)	21.4	120	80	80	7.13	42.8	14.3
Center Frequency (MHz)	10.7	60	20 (60*)	20 (100*)	10.7	10.7	10.7
Bandwidth (MHz)	0.2	0.2	0.27/3.84	0.27/3.84	0.2	0.2	0.2
OSR	107	600	148/10	148/10	36	107	36
Dynamic Range (dB)	N/A	N/A	84/46	86/50	62	74	67
Peak SNDR (dB)	42.3	72	72/42	78/46	59.5	61	59

"*" denote input frequency

can be seen that such bandpass ΣΔMs can achieve robust narrowband performance, but only at low IF because of the settling errors of SC resonators/filters at higher frequencies. For high IF digitization, CT bandpass ΣΔM is preferred.

2.2.2 CT Single-loop, Single-bit Bandpass ΣΔMs

In CT bandpass ΣΔMs, the CT loop filters can be realized using active-RC [27][33], Gm-C [22][24][28][30][31][34][35] and LC resonators/filters [23][25][26]. Most of them are designed from DT prototypes by using the impulse-invariant DT-to-CT equivalence introduced in section 2.1.8. Compared with DT bandpass ΣΔMs, CT bandpass ΣΔMs are able to work at much higher center frequencies.

Active-RC resonators have been used to implement high-order bandpass ΣΔMs. A CMOS 6^{th}-order ΣΔM was designed for AM/FM narrowband application centered at 10.7-MHz IF. It achieves a 63.5-dB SNDR in 200-kHz bandwidth. However, its center frequency must be tuned manually, which is not desirable in practical narrowband

application. A wideband 10^{th}-order ΣΔM with quite impressive performance is presented in [33]. So far it is the highest order single-loop bandpass ΣΔM ever reported. But it was implemented in a costly InP process and consume huge power (6W).

The active resonator can also be implemented with Gm-C circuit. Compared with active-RC resonators, Gm-C resonators can operate at much higher frequency. CT bandpass ΣΔMs based on Gm-C resonators are designed for both narrowband [30] and wideband [34] applications with high IF around 200MHz. The ΣΔM reported in [30] achieve only 68-dB SNDR in 200-kHz signal band, which is about 10dB lower than the state-of-art DT bandpass ΣΔM, even with large OSR (2000). The low Q of Gm-C resonator and clock jitter noise may account for the limited performance. The ΣΔM in [34] achieves good wideband performance (SNDR of 78dB in 1-MHz, and 50dB in 60-MHz signal band), but at the cost of large power consumption since it is realized in AlInAs/InGaAs process.

The center frequencies of CT bandpass ΣΔMs can be further pushed into gigahertz

Table 2.2 Summary of CT single-loop, single-bit bandpass ΣΔMs

Design	[27]	[33]	[22]	[30]	[34]	[25]	[26]
Technology (μm)	0.5/ CMOS	InP	AlInAs/ InGaAs	SiGe	AlInAs/ InGaAs	0.5/ Bipolar	0.5/ SiGe
Supply Voltage (V)	5/3.3	N/A	N/A	3	±5	5	5
Type	Active-RC	Active-RC	Gm-C	Gm-C	Gm-C	LC	LC
Modulator Order	6	10	2	4	4	2	4
Power (mW)	60	6000	1400	64	3200	135	350
Sampling Frequency (MHz)	40	2500	4000	800	4000	3800	4000
Center Frequency (MHz)	10.7	90	55.5	200	140~210	950	1000
Bandwidth (MHz)	0.2	25	0.366/62.6	0.2	1/60	0.2	4
OSR	100	50	5464/32	2000	2000/33	9500	125
Dynamic Range (dB)	67	N/A	80/48	N/A	N/A	N/A	62
Peak SNDR (dB)	63.5	74	92/44	68	78/50	49	53

range by employing integrated passive LC resonators as loop filters. However, their performance is quite poor compared with active-RC and Gm-C resonators based ΣΔMs. The main reason is that the Q factor of the integrated LC resonator is very low, which greatly degrades the performance of the ΣΔM.

Some CT bandpass ΣΔMs employing active-RC, Gm-C and LC resonators are listed in Table 2.2. Most of them are realized in SiGe or III-V process and consume significant power. In general, the limited Q of CT resonator and shift of the center frequency due to the PTV may limit the performance, especially for narrowband applications.

2.2.3 Cascade and Multi-bit Bandpass ΣΔMs

For single-loop bandpass ΣΔMs, it has been shown that increasing the order of the ΣΔM may result in stability problem. High-order (≥ 6) bandpass ΣΔMs can also be realized by cascading two or more low-order (2^{nd}- or 4^{th}- order) bandpass ΣΔM stages [64]. High-order noise shaping is achieved without stability problem, since the constituent low-order ΣΔMs are intrinsically stable [38]. The concept of the cascade ΣΔM is illustrated in Figure 2.23. The input to the first ΣΔM is the input signal of the entire ΣΔM. The consecutive ΣΔMs modulate the quantization noise from their previous modulator. The digital outputs of all the stages are combined with the proper digital cancellation logic which cancels the quantization noise from proceeding stages. The only quantization noise that remains visible at the output is from the last stage, which is shaped by all the loop filers in the cascade ΣΔM. High order ΣΔM is therefore realized.

Cascade bandpass ΣΔMs are able to achieve high resolution with low OSR, but they have their own drawback. The mismatch of the transfer functions between the analog loop filters and digital cancellation block results in the imperfect cancellation of quantization noises, which allows the lower-order shaped quantization noise to leak to the output of the ΣΔM, and hence degrades the SNR. So far all the published cascade

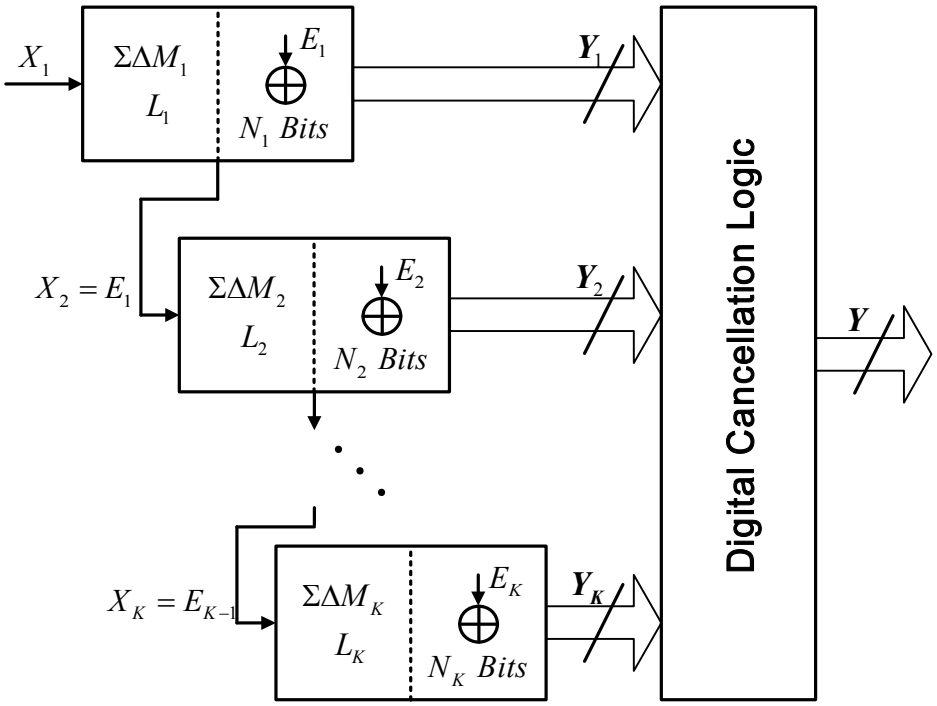


Figure 2.23 Conceptual cascade ΣΔM

bandpass ΣΔMs are based on SC circuits [13][15][18][20][65] because of the relatively good matching between SC loop filters and digital circuits. No CT cascade bandpass ΣΔM was reported.

All bandpass ΣΔMs discussed so far employ single-bit quantizer. Single-bit quantizer is frequently employed because of its simplicity and inherent linearity. Bandpass ΣΔMs can also be realized with multi-bit quantizer, which has less quantization noise and hence improves the overall ΣΔM's resolution. Since the multi-bit quantizer has well defined gain, therefore the stability of the multi-bit ΣΔM is more predictable [38]. Furthermore, it will be shown in section 3.4.4 that clock jitter noise of multi-bit DAC is less than that of single-bit DAC in CT ΣΔMs. However, these benefits are achieved at the expense of higher circuit complexity and power consumption. Another main disadvantage of the multi-bit ΣΔM is that the non-idealities in the multi-bit feedback DACs, such as nonlinearity, can not be shaped by loop filter. Various

Table 2.3 Summary of cascade and multibit bandpass ΣΔMs

Design	[13]	[15]	[20]	[81]	[82]	[83]	[84]
Technology (μm)	0.8/ CMOS	0.35/ CMOS	0.18/ CMOS	0.35/ BiCMOS	0.18/ CMOS	0.18/ CMOS	0.25/ CMOS
Supply Voltage (V)	3	3	1.8	3.1	1.8	1.8	2.5
Type	SC/4-2 cascade/ Sub-sampling	SC/4-4 cascade/ Sub-sampling	SC/2-2-2 cascade/ 2path	LC+RC+ SC hybrid	Active-RC	SC	SC/2-2 cascade
Quantizer resolution (bits)	1	1	1	3	4	5	3
Modulator Order	6	8	6	6	2	2	4
Power (mW)	7	37	150	50	2.2	88	77
Sampling Frequency (MHz)	13	80	60	32	48	37.05	10
Center Frequency (MHz)	3.25 (81.25*)	20 (60*)	40	4	2	10.7	0.566
Bandwidth (MHz)	0.2	1.25/1.762	2.5	0.333	1	0.2	0.25
OSR	32.5	32/23	24	48	24	92.6	20
Dynamic Range (dB)	72	82/72	N/A	90	68	78	79
Peak SNDR (dB)	63	75/69	69	77	64	72	77

"*" denote input frequency

techniques, mostly originated in lowpass multi-bit ΣΔMs, have been proposed to overcome the DAC nonlinearity, such as element trimming [38], digital calibration technique [66-68], dual-quantization technique [69][70], self-calibration technique [71-73], dynamic element matching (DEM) techniques [74-80]. Among them, DEM is most frequently used.

Some efforts have made to implement DT [15][83][84], CT [32][82] and hybrid (LC+RC+SC) [81] bandpass multi-bit ΣΔMs. Most of them can only work at low IF (<40MHz), except the CT ΣΔM in [32], but the DAC nonlinearity was not well treated.

Some recently published cascade and multi-bit bandpass ΣΔMs are summarized in Table 2.3. Design of cascade and multi-bit bandpass ΣΔMs with higher center frequency and robust performance still remains a challenge for today's circuit designers.

2.3 Limitations of the Resonators in Conventional Bandpass ΣΔMs

In bandpass ΣΔMs, the integrators in lowpass ΣΔMs are replaced by resonators. The main limitations of the resonators are the low quality factor Q and resonant frequency variation, which have direct impact on the overall performance of the bandpass ΣΔM.

The performance degradation of the bandpass ΣΔMs caused by limited Q factor of the resonators is similar to the degradation due to the finite DC gain of the integrators in the lowpass ΣΔMs, both decrease the SNR and cause serious tone problem at output of the modulator [51]. The effect of limited Q on the SNR performance is studied by Matlab simulation for a 2nd-order CT bandpass ΣΔM (f_s=80MHz, f_c=20MHz, f_B=200kHz, OSR=200), and the result is shown in Figure 2.24. Clearly, the SNR degradation is significant when Q is less than 200. A good rule of thumb for Q needed is given by Q > OSR [51]. On the other hand, the change of resonant frequency also degrades the SNR, since it shifts the notch away from the center signal frequency and hence increases the overall in-band noise. Normally, the resonant frequency variation should be less than 20% of signal bandwidth [85].

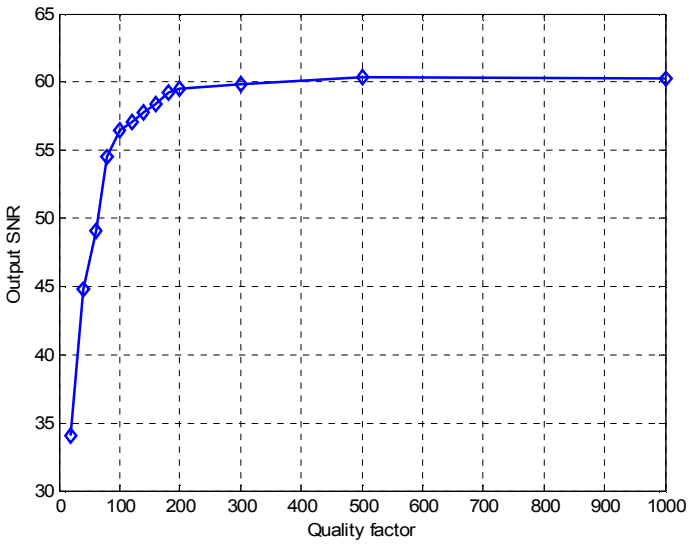


Figure 2.24 SNR degradation due to Q (OSR=200)

Various resonators have been used in bandpass ΣΔMs, which include SC resonator in DT domain and active-RC, Gm-C, LC resonators in CT domain. In general, DT SC resonators can achieve quite large Q factor (>200) and good center frequency accuracy, but only at low IF frequencies (usually <50MHz). Active Gm-C and active-RC resonators can work in higher frequencies (up to 200MHz) but suffer from low Q and variation of the resonant frequency. Integrated passive LC resonators usually find their application in gigahertz range. However, they also have poor Q factor and their resonant frequencies are sensitive to the variation of inductance and capacitance values. In the following subsections, various DT and CT resonators are discussed in detail, as well as their performance limitations.

2.3.1 DT SC Resonators

A DT SC resonator in bandpass ΣΔMs, mostly centered at $f_s/4$, with transfer function given by

$$H_{res}(z) = \frac{z^{-2}}{1+z^{-2}} \; or \; \frac{z^{-1}}{1+z^{-2}} \tag{2.42}$$

can be realized with different circuit structures [7]. The commonly used implementations are Forward Euler (FE) [7][10], lossless discrete integrator (LDI) [7][11][12][16] and double-delay (DD) [13-15][17-19][21][86]. The FE structure consists of two identical integrators with two feedback paths b1 and b2, as shown in Figure 2.25. Both integrators have one sampling period delay. The transfer function of the FE resonator is

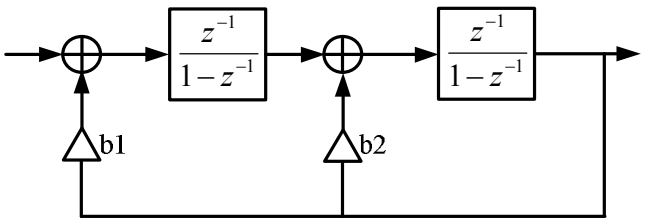


Figure 2.25 Forward Euler resonator structure

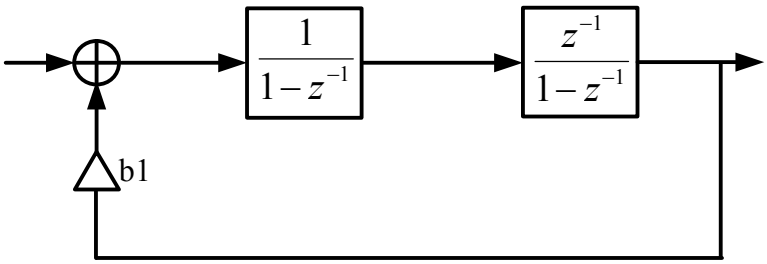


Figure 2.26 Lossless discrete integrator resonator structure

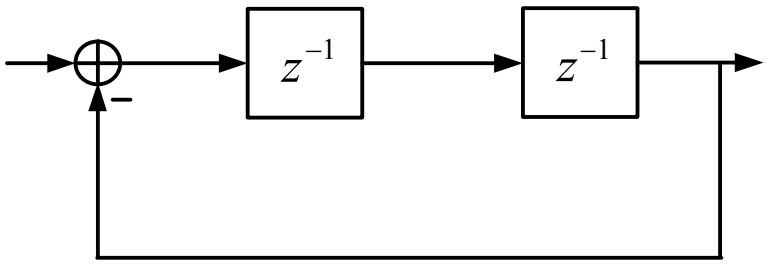


Figure 2.27 Double delay resonator structure

$$H_{res\_FE}(z) = \frac{z^{-2}}{1-(2+b2)z^{-1}+(1-b1+b2)z^{-2}} \tag{2.43}$$

For b1=b2=-2, the center frequency can be set at $f_s/4$. The LDI resonator, given in Figure 2.26, also consists of two integrators, but one is delay-free and the loop has only one feedback coefficient b1. The transfer function can be expressed by

$$H_{res\_LDI}(z) = \frac{z^{-1}}{1-(2+b1)z^{-1}+z^{-2}} \tag{2.44}$$

The center frequency is at $f_s/4$ if b1=-2. The DD resonator in Figure 2.27 is realized by two serially-connected delay elements and a feedback path. The transfer function is given as

$$H_{res\_DD}(z) = \frac{z^{-2}}{1+z^{-2}} \tag{2.45}$$

Unlike FE and LDI resonators, the center frequency of DD resonators is fixed at $f_s/4$ and can not be varied.

Ideally, these three resonators are identical with proper choice of feedback coefficients. However, they behave quite differently when the circuit non-idealities are taken in account. For example, if only the capacitor mismatch ε_c is considered (for the sake of simplicity, the same gain error is assumed for both signal and feedback paths), the transfer functions in (2.43-2.45) need to be modified to (2.46-2.48), respectively.

$$H_{res\_FE}(z) = \frac{(1+\varepsilon_c)^2 z^{-2}}{1-\left(2+(1+\varepsilon_c)b2\right)z^{-1}+\left(1-(1+\varepsilon_c)^2 b1+(1+\varepsilon_c)b2\right)z^{-2}} \tag{2.46}$$

$$H_{res\_LDI}(z) = \frac{(1+\varepsilon_c)^2 z^{-1}}{1-\left(2+(1+\varepsilon_c)^2 b1\right)z^{-1}+z^{-2}} \tag{2.47}$$

$$H_{res\_DD}(z) = \frac{(1+\varepsilon_c)^2 z^{-2}}{1+z^{-2}} \tag{2.48}$$

For the FE resonator in (2.46), the accuracy of the resonant frequency (determined mainly by the coefficient of z^{-1} term) and Q factor (determined mainly by the coefficient of z^{-2} term) are both dependent on the gain error ε_c. Thus, FE resonator is less favorable for the bandpass ΣΔMs. Compared with FE resonator, LDI resonator is less sensitive to the gain error for its Q factor, but more sensitive for its resonant frequency accuracy. For the DD resonator, its resonant frequency and Q factor are almost unaffected. Therefore, DD resonator is the preferable structure for the realization of high-performance bandpass ΣΔMs with center frequency of $f_s/4$. Another advantage of the DD resonator is that, instead of using two analog delay elements in series [17][18], it can be implemented with a pseudo-two-path structure [13][14][19][21][86], in which the number of the opamps can be reduced to one. A 4th-order modulator (consists of two resonators) employing only one opamp has also been reported [15]. As for the FE and LDI topologies, they require at least two opamps and therefore large power consumption.

In addition to the capacitor mismatches, the non-idealities of the opamp (such as the finite DC gain and the bandwidth) also affect the performance of the resonator. The effects of non-ideal opamps on different resonator topologies have been studied extensively [7][9][14][17]. One of major bottlenecks in the SC resonators is the speed of opamp, whose unity-gain bandwidth is normally required to be 5-10 times of the sampling frequency, depending on the settling error. This restricts the sampling frequencies of the SC resonators to about 200MHz in today's CMOS processes with reasonable large power consumptions. Thus, for $f_s/4$ bandpass ΣΔMs, the center frequency of IF is normally below 50MHz. To digitize high IF signal and alleviate the requirement on the bandwidth of opamp, two techniques, namely sub-sampling [13-15] and double-sampling [16-21], have been employed in DT bandpass ΣΔMs.

Sub-sampling means that a signal is sampled at a frequency lower than the Nyquist rate. It is well known that sampling signals at frequencies lower than the Nyquist rate will cause aliasing problem. For narrowband IF signals, the aliasing problem can be prevented if the sampling frequency is much higher than the signal bandwidth [13]. Therefore, sub-sampling technique can be used at the input of the DT bandpass ΣΔM to down-converted the signal to lower IF (< 20MHz) before it is quantized, and the bandwidth requirement for opamps can be relaxed. However, sub-sampling technique has its own drawbacks [13]. First of all, the wideband noise as well as some unwanted signals can be aliased and appear in the signal band and thus corrupt the signal. Secondly, it makes the ΣΔM more sensitive to the jitter noise from the sub-sampling clock. Therefore, the inherently higher noise figure and large susceptibility to jitter noise make sub-sampling techniques less favorable for application with IF higher than 100MHz. Most of the reported sub-sampling DT bandpass ΣΔMs work with the input signal frequencies ranging from 80MHz to 100MHz [13-15][18].

In double-sampling SC resonators, the opamps are used during both phases of the clock. Hence, double-sampling technique increases the effective sampling frequency by a factor of two without the need of the high-speed opamp. In double-sampling SC resonators, most of the circuits need to be duplicated and thus circuit complexity increases. So far, the highest effective sampling frequency reported in the DT bandpass ΣΔMs is 240MHz in an $f_s/4$ design [16]. A major limitation of the double-sampled SC resonator is the mismatch in the two sampling paths that causes an in-band image of the input signal. Both sub-sampling and double-sampling can be employed in the same design [18].

2.3.2 Active CT Resonators: Active-RC and Gm-C

A CT active resonator (biquad filter) can be realized with two cascade integrators with a feedback loop around them, as shown in Figure 2.28. The output of the resonator can be taken from the output of either integrator. The resultant transfer functions are given by

$$\frac{V_{o1}(s)}{V_{in}(s)} = \frac{\omega_0 s}{s^2 + \omega_0^2} \tag{2.49}$$

and

$$\frac{V_{o2}(s)}{V_{in}(s)} = \frac{\omega_0^2}{s^2 + \omega_0^2} \tag{2.50}$$

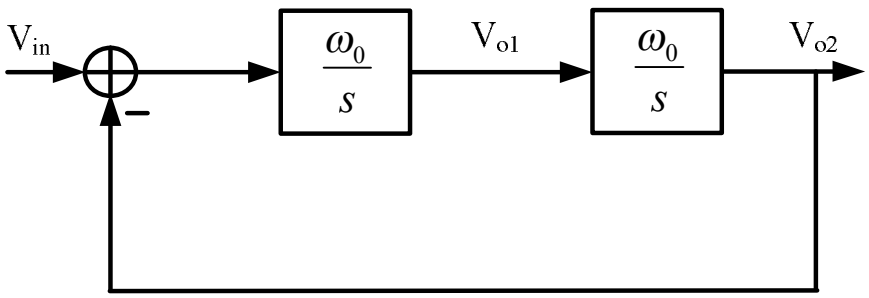


Figure 2.28 A CT active resonator with two integrators

where ω_0 is the unity-gain frequency of the integrator and also the resonant frequency. Note that (2.49) and (2.50) are derived with ideal integrator whose transfer function is $T(s)=\omega_0/s$. However, the transfer function of a practical integrator is $T(s)=\omega_0/(s+\omega_1)$, in which $\omega_1 << \omega_0$ is a nonzero dominant pole frequency of the integrator. (2.49) and (2.50) should be, respectively, modified to

$$\frac{V_{o1}(s)}{V_{in}(s)}=\frac{\omega_0(s+\omega_1)}{s^2+2\omega_1 s+(\omega_1^2+\omega_0^2)}\approx\frac{\omega_0 s}{s^2+\frac{\omega_0}{Q}s+\omega_0^2} \tag{2.51}$$

and

$$\frac{V_{o2}(s)}{V_{in}(s)}=\frac{\omega_0^2}{s^2+2\omega_1 s+(\omega_1^2+\omega_0^2)}\approx\frac{\omega_0^2}{s^2+\frac{\omega_0}{Q}s+\omega_0^2} \tag{2.52}$$

where $Q=\omega_0/2\omega_1$ is the quality factor.

Figure 2.29 and Figure 2.30 show the typical active-RC and Gm-C implementations of (2.51), respectively. For the active-RC resonator, $\omega_0=1/RC$ and $\omega_1=(1/RC)\cdot(1/A)$, A is the finite DC gain of the non-ideal opamp. Similarly for Gm-C resonator, $\omega_0=G_m/C$ and $\omega_1=G_o/C$, in which G_m is the transconductance and G_o is the nonzero

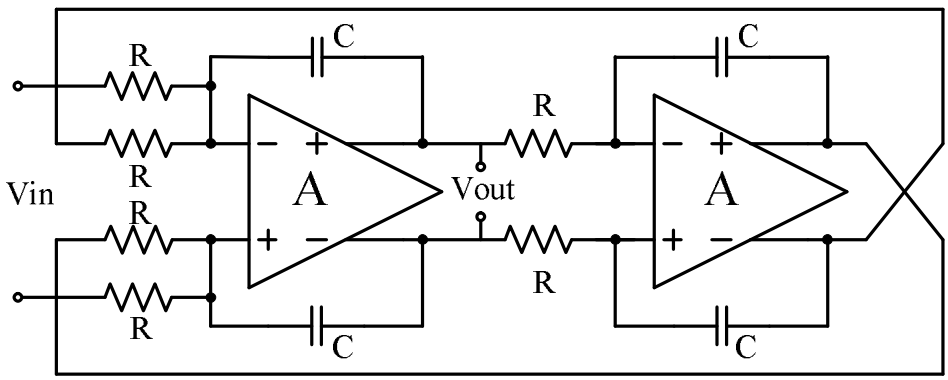


Figure 2.29 Active-RC resonator

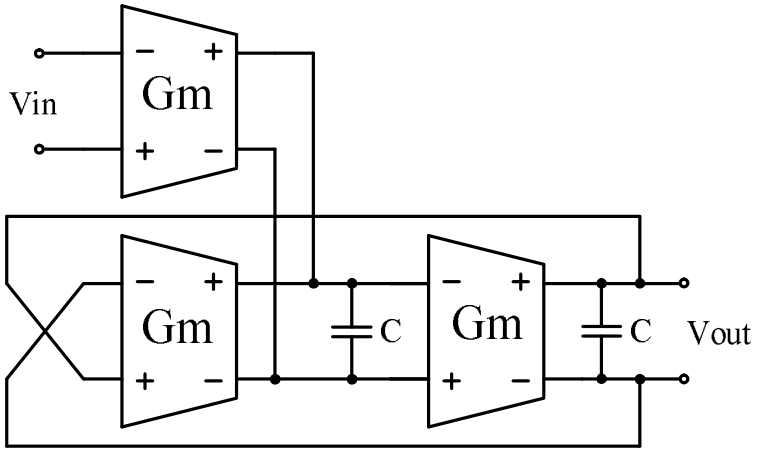


Figure 2.30 Gm-C resonator

output conductance of the transconductor.

In the active-RC resonator, $Q = \omega_0 / 2\omega_1 = A/2$, therefore, with carefully designed opamp gain, a reasonable Q can always be guaranteed [27][33]. However, this is not the case in Gm-C resonator, in which $Q = \omega_0 / 2\omega_1 = G_m / (2G_o)$, especially when the resonant frequency is high. This is because in high-frequency transconductor, the output impedance $R_o = 1/G_o$ can not too high and is normally in the range of several hundred to several thousand ohms, which restricts the achievable Q below 30 [30]. The limited Q will degrade the performances of the CT bandpass ΣΔMs. In order to achieve a high Q, the finite output impedance of the transconductor can be compensated by employing an extra transconductor configured as a negative resistor in the resonator loop [87][88]. However, voltage headroom is reduced due to the additional negative transconductor and the resultant Q is very sensitive to the process variation since the negative resistance is subject to the process variation [30]. A more robust approach is to use two-stage Gm-C-opamp integrator [30][31][34], as shown in Figure 2.31. The left side is a conventional Gm-C integrator and the right side is a Gm-C-opamp integrator. It is easy to prove that the Q of Gm-C-opamp resonator equals to $A \cdot G_m / (2G_o)$, where A is the DC gain of the

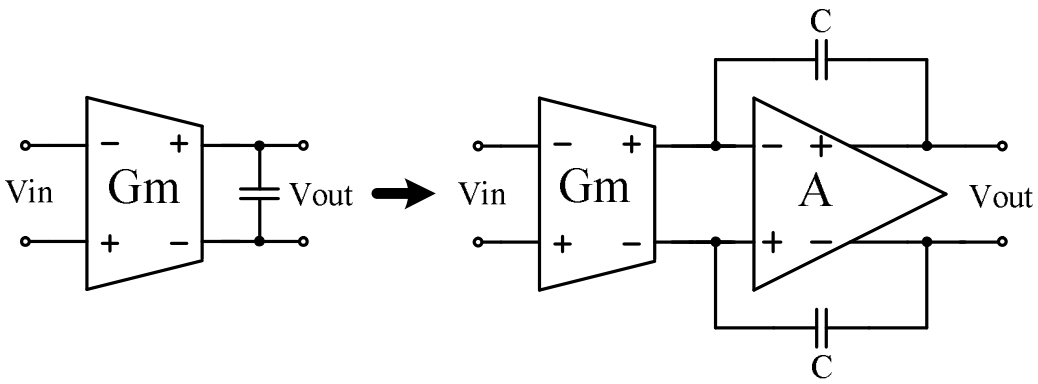


Figure 2.31 Gm-C-opamp integrator

opamp. The Q improvement is achieved at the expense of the large power consumption due to the additional opamps.

In active-RC and Gm-C resonators, the center frequencies are given by $\omega_0 = 1/RC$ and $\omega_0 = G_m/C$, respectively. Since the on-chip resistors, capacitors and transconductors typically have tolerance larger than 30%, the center frequencies of the active resonators are poorly controlled unless frequency tuning is employed. However any tuning method will increase the circuit complexity and power consumption. Even with the help of frequency tuning, the resonant frequency tolerance can only be improved to 1%-5%, which may not still be enough for narrowband digitization at high center frequency.

2.3.3 Passive CT LC Tank Resonator

A CT resonator can also be implemented with a LC tank, as shown in Figure 2.32. An input transconductor is used to convert the input voltage to current, and drives the LC tank. In ideal case, the resultant transfer function is given by,

$$\frac{Vout}{Vin} = \frac{\frac{G_m}{C}s}{s^2 + \frac{1}{LC}} \tag{2.53}$$

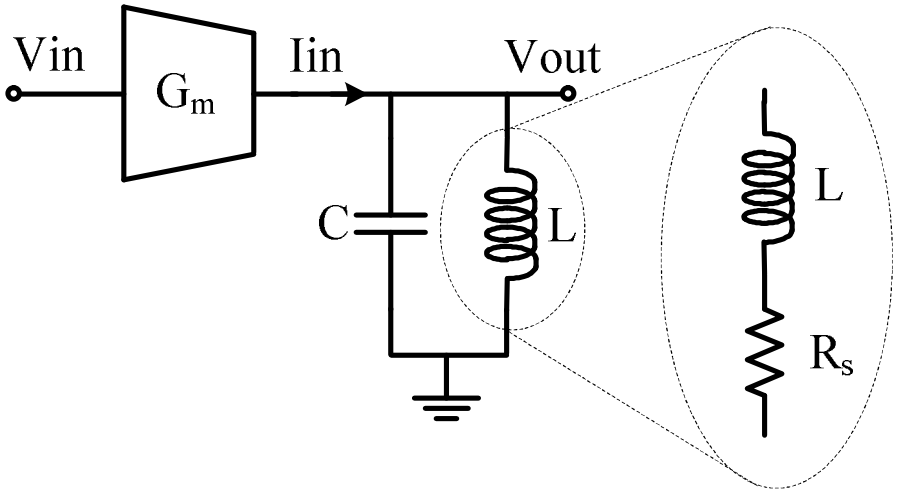


Figure 2.32 LC tank resonator

It appears to be a very good resonator with infinite Q. However, the integrated on-chip spiral inductor has large parasitic resistance, which makes the spiral inductor quite lossy and has poor quality factor. For a lossy inductor, the transfer function in (2.61) should be modified to

$$\frac{Vout}{Vin} = \frac{\frac{G_m}{C}s + \frac{R_s}{LC}}{s^2 + \frac{R_s}{L}s + \frac{1}{LC}} \tag{2.54}$$

The Q factor of the resonator is $\sqrt{L/C}\big/R_s$. A large L is preferred to guarantee a high Q factor. However, huge silicon area consumption makes the inductance of a reasonable integrated spiral inductor normally less than 10-nH. Therefore, the achievable Q factor of the LC resonator is typically around 5-10 [25]. Furthermore, the limited inductance makes the LC tank resonator only suitable for applications in gigahertz range. Q enhancement circuit, which is similar to negative resistor approach in Gm-C resonators, has been used to increase the Q factor [25][51]. However, it deteriorates the linearity of the LC resonator, since the negative resistor is realized by transconductor which is difficult to be designed with high linearity in gigahertz range.

2.4 Why Electromechanical Resonators

There are three main considerations which motivate us to employ electromechanical resonators in CT bandpass ΣΔMs.

First of all, in conventional CT bandpass ΣΔMs, all loop filter coefficients are implemented by either RC or LC product or G_m/C ratio. Their values are subject to process and temperature variation. The accuracy of their parameters is typically from 20% to 30%. Therefore, frequency tuning/calibration is always needed for CT bandpass ΣΔMs, especially in narrowband applications. Electromechanical resonators, including crystal, SAW, BAW and MEMS resonators, on the other hand, possess the features of accurate center frequency (typical tolerance less than 0.1% depending on the design and process) and good temperature stability (a few to several tens of ppm/°C; for MEMS resonators, proper temperature compensations may be needed), and thus do not require frequency tuning.

Secondly, the performance of CT bandpass ΣΔMs based on both LC and Gm-C resonators suffer from the low Q factors. The low Q of LC resonator is mainly due to the losses from series resistance of the conductor used to implement on-chip integrated inductors and magnetically induced eddy current in the substrate. The Q degradation in the Gm-C resonator, on the other hand, is because of its finite output impedance. Both become much severer at high frequencies. Although Q enhancement techniques can be explored [24][25][29], they only provide limited improvement at the expense of linearity degradation. The electromechanical resonators are well known to have high Q factor, typically greater than 1000. Therefore, they can overcome the weakness of the conventional resonators and are good candidates to replace LC and Gm-C resonators in CT bandpass ΣΔMs. Some electromechanical resonators, such as MEMS and BAW, can

be realized on silicon today. Thus, the electromechanical resonator based bandpass ΣΔM can be made in either monolithic or hybrid form.

Furthermore, electromechanical resonators with wide resonant frequency range are available from several thousand hertz to a few gigahertz. This makes it possible to realize the CT bandpass ΣΔMs for extensive applications that require different center frequencies.

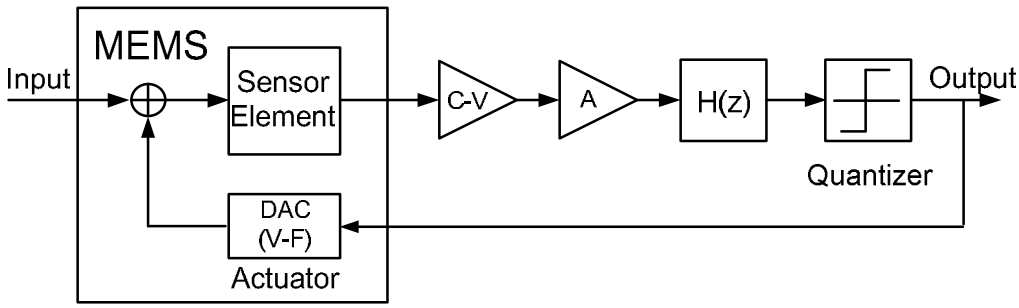


Figure 2.33 Block diagram of MEMS sensor employing ΣΔ modulation

2.5 Existing Electromechanical ΣΔMs

Recently, ΣΔ modulation has been employed in the interface circuits for the micro-machined inertial sensors, such as accelerometers [89-95], gyroscopes [96] and pressure sensors [97]. A typical block diagram of such systems is shown in Figure 2.33. The MEMS sensor element is mainly used as a transducer to sense the input signal, which is non-electrical, and convert it to an electrical one. Electronic loop filter is still needed for the realization of ΣΔ modulation. Although these systems sometimes bear the name of electromechanical ΣΔMs, they are essentially different from the conventional stand-alone ΣΔMs. Since the input signal is not in electrical domain, thus more accurately, they are the smart sensors.

CHAPTER 3

CT BANDPASS ΣΔM BASED ON ELECTRO-MECHANICAL RESONATOR

This chapter presents the design of continuous-time bandpass ΣΔMs based on electromechanical resonators. A brief introduction to electromechanical resonators is given at the beginning. Issues pertaining to the realization of electromechanical resonators based CT bandpass loop filters are then discussed. Finally, structures of the ΣΔMs are proposed. Some non-idealities involved in implementation of CT ΣΔMs are also analyzed.

3.1 Introduction to Electromechanical Resonators

Electromechanical resonators and filters involve a form of mechanical wave propagation at some stage between their input and output terminals. Generally, there are four kinds of electromechanical resonators, namely crystal, ceramic, surface or bulk acoustic wave (SAW or BAW) and MEMS resonators.

- **Crystal resonators** are electromechanical resonators that use quartz as the solid medium in which mechanical vibrations take place. The quartz elements are piezoelectric, and the acoustic energy is distributed throughout the resonator in so-called bulk waves (as opposed to surface waves).
- **Ceramic resonators** are similar to crystal resonators except that the piezoelectric lead-zirconate-titanate (PZT) material is usually used in the place of quartz. Their

Table 3.1 Summary of different electromechanical resonators

	Resonant Frequency (f_C)	Quality Factor (Q)
Crystal	$\leq$ 500MHz	$\geq$ 20,000
Ceramic	10kHz – 100MHz	500-1000
SAW/BAW	20MHz – 3GHz	$\geq$ 2,000
MEMs	1MHz – 1.5GHz	$\geq$ 2,000 (under certain vacuum condition)

Q factors are lower than those of crystal resonators, but they are generally cheaper and smaller than crystal resonators.

- **SAW or BAW resonators** use various solid medium such as quartz, lithium tantalate, lithium niobate, zinc oxide, and PZT ceramics. The vibration energy in SAW resonators is in the form of acoustic wave near the surface of the medium. In contrast to SAW, BAW resonators use bulk acoustic waves.
- **MEMS resonators** are fabricated using micromachining technique mainly on silicon substrate. The mechanical microstructure is driven by static electric force to form a resonant device.

Table 3.1 summarizes the resonant frequencies and quality factors of different types of resonators. In this thesis, SAW and MEMS resonators will be used.

3.1.1 SAW Resonators

SAW resonators are widely used in oscillators and filters of wireless communication systems [98][99]. High-Q factor and low power consumption are their main advantages. SAW resonators can be configured electrically as one-port or two-port networks. Their operations are based on the judicious use of SAW reflection grating to form resonant structures.

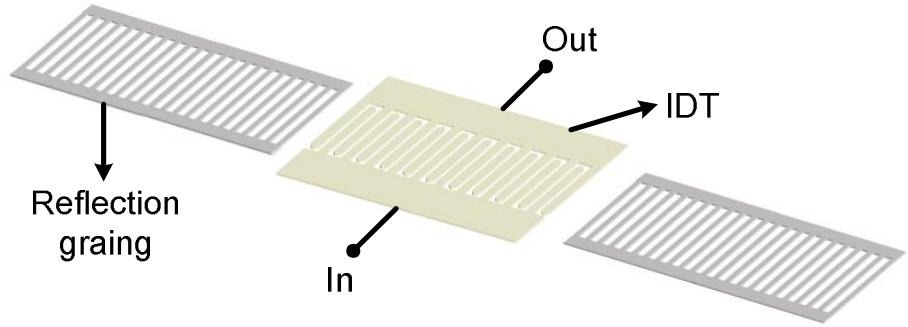


Figure 3.1 One-port SAW resonator

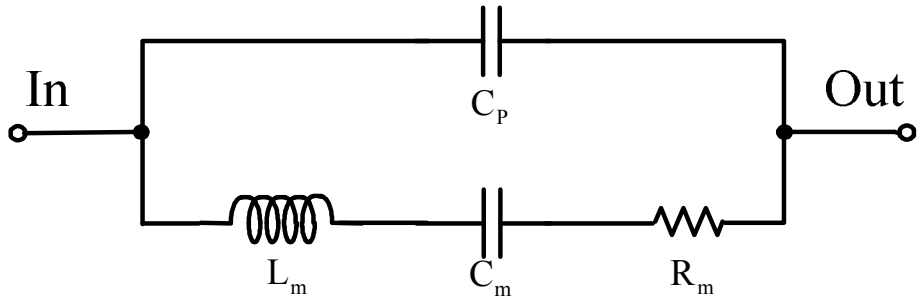


Figure 3.2 Equivalent circuit of one-port SAW resonator

Figure 3.1 shows a typical structure of one-port SAW resonator. This resonator is made on a piezoelectric substrate using an interdigital transducer (IDT) in between two SAW reflection gratings. The gratings are arrays of metal strips with spacing λ/2 (λ is the wavelength of the acoustic wave). The resonator has two gratings that form a resonant cavity, with an IDT in the cavity to couple it to the electrical terminals, as shown in Figure 3.1. The equivalent lumped-element circuit is given in Figure 3.2. C_p represents the static capacitance of IDT, while L_m, C_m, and R_m relate to equivalent motional parameters for the series-resonance condition. For example, the one-port SAW resonator is normally employed in fixed frequency oscillator as traditional crystal resonator does, but at much higher frequencies.

Compared with their one-port counterpart, two-port SAW resonators are more flexible in terms of design constraints and can be used to implement oscillators with either fixed or tunable frequency. A typical structure of two-port SAW resonator is

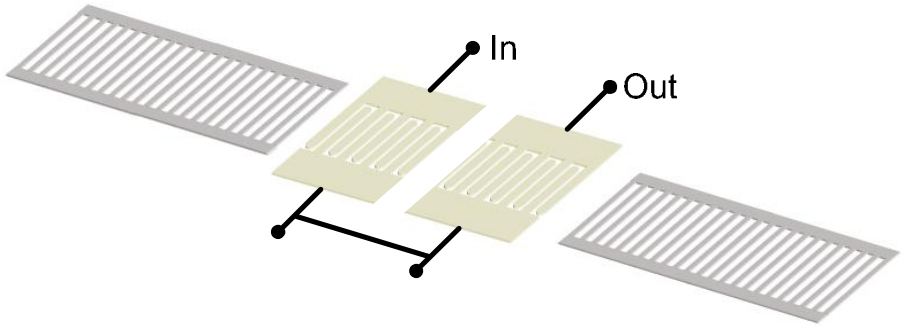


Figure 3.3 Two-port SAW resonator

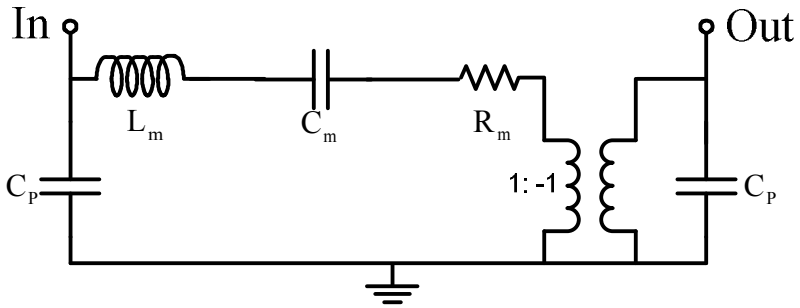


Figure 3.4 Equivalent circuit of two-port SAW resonator

depicted in Figure 3.3. There are two identical IDTs in two-port resonators. Figure 3.4 shows the LCR lumped equivalent circuits. The voltage transfer function between input and output IDTs may be considered to be composite of two contributions. In the absence of reflection gratings, it would just be that for a simple SAW filter with uniform and equal input and output IDTs. With the reflection grating included, the resonator response will superimpose on the filter's response around the center frequency [98]. The underlying filter response will limit the dynamic range of the overall resonator. Our designed bandpass ΣΔMs will mainly employ one-port SAW resonator.

3.1.2 MEMS Resonators

Recently, with the rapid development of silicon micromachining technologies, MEMS resonators have found their applications in miniaturized high-frequency filters [100] and reference oscillators [101][102]. Furthermore, polycrystalline silicon MEMS

resonators, which are fabricated with surface micromachining technology, can be integrated with conventional CMOS/BiCMOS circuits. A fully monolithic channel filter with high center frequency and good shape factor and a fully monolithic high-Q oscillator can be implemented to potentially replace offchip SAW and crystal devices.

In MEMS resonators, the micro-scale mechanical elements and integrated transducers convert the motion of the mechanical elements into an electrical signal and vice versa. Various physical structures having mechanical resonance at specific frequencies have been proposed. Among them, capacitively transduced clamped-clamped beam (CC-beam) resonator and wine glass disk resonator are the preferred choices because of their relatively high Q factor and temperature stability at higher frequencies [102].

CC-beam MEMS resonators are attractive for low cost application, since they can be realized in polysilicon surface micromachining process with only a few masks. Figure 3.5 depicts a perspective view schematic of a CC-beam resonator, together with a typical one-port bias and excitation scheme. As shown, the CC-beam resonator is comprised of a polysilicon beam (anchored to the substrate at its end) and an input electrode which is centrally located under the beam. A DC voltage V_P is applied to the conductive beams to

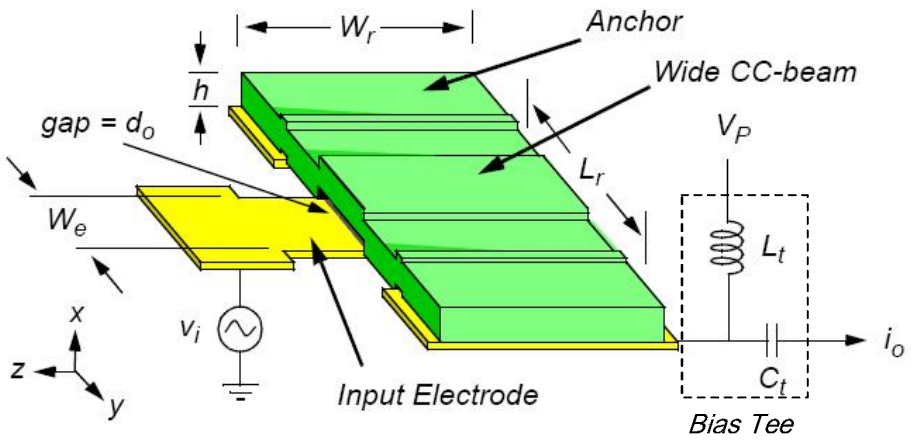


Figure 3.5 CC-beam MEMS resonator [102]

excite it and drive it closer to the input electrode with static electric force. Meanwhile, the ac input voltage signal v_i is applied to the underlying input electrode. The combination of V_P and v_i generates a time-varying electric force that drives the beam into mechanical resonance when the frequency of v_i equal to the beam's natural frequency. Note that the output signal is in current mode and can be sensed with simple resistor load or with transimpedance amplifier. The lumped equivalent circuit of CC-beam resonator is similar to that of one-port SAW resonator given in Figure 3.2. The values of the motional elements are determined by the stiffness and mass of the resonator, and the magnitude of the electromechanical coupling at its transducer electrode. The C_P in CC-beam MEMS resonator indicates the static overlap capacitance between the beam and input electrode. The power-handling capability of the normal CC-beam MEMS resonator is limited by its quite large motional resistance R_m (several thousand ohms) and can be improved to about several hundred ohms by widening the width of the CC-beam [102]. The resonant frequency of the CC-beam resonator can be increased effectively by shortening the length of its beam. However, the Q factor will also decrease as beam length shrinks. So far, the reported CC-beam resonator with the highest resonant frequency is 92MHz [103].

The extensional vibrating disk geometry can be used to realize very high frequency resonator. Figure 3.4 depicts the perspective view schematic of a disk resonator operating in wine-glass-mode. The disk is supported by two beams attached to it and surrounded by four electrodes with lateral electrode-to-disk air/solid gap. The disk can expand along one axis and contract in the orthogonal axis. A DC bias voltage V_P is still needed, as in the CC-beam resonator, to bias the disk structure. Note in this disk resonator, the input and output are connected to two separated electrodes, not to the disk directly. Therefore, V_P can be applied to the disk directly without the need for bias tee to

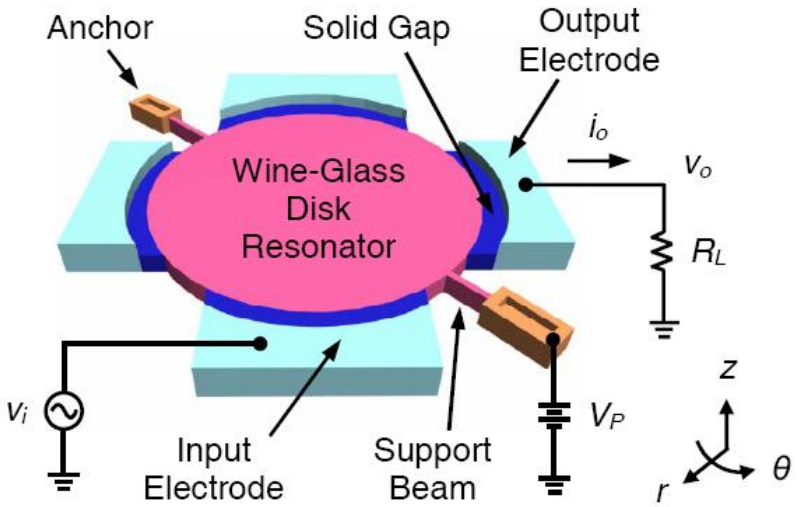


Figure 3.6 Wine-glass disk MEMS resonator [102]

separate DC and AC signals. The wine glass disk resonator is inherently a two-port device and its equivalent circuit is given in Figure 3.7. The static capacitance C_P no longer connects input and output, but is shunted to the ground by the DC biased disk structure. Other than wine-glass mode, radial mode is preferred in the design of even higher frequency disk resonators. A radial-mode diamond disk resonator was implemented with Q>10,000 at frequency exceeding 1.5GHz [104]. Even for polysilicon based design, a disk resonator with resonant frequency of 1.2-Hz has been reported [105].

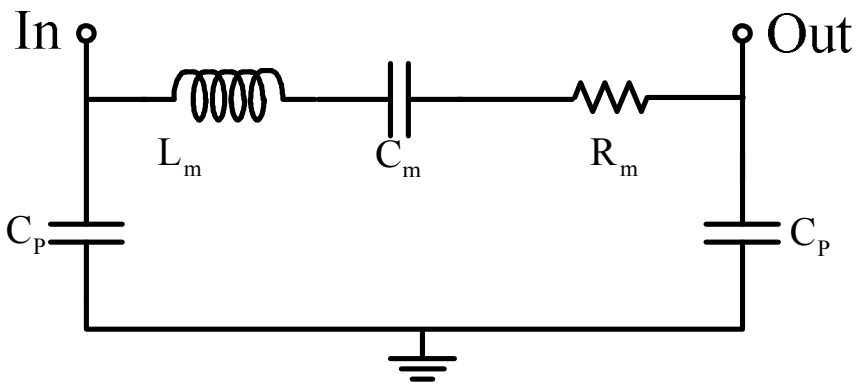


Figure 3.7 Equivalent circuit of wine glass disk MEMS resonator

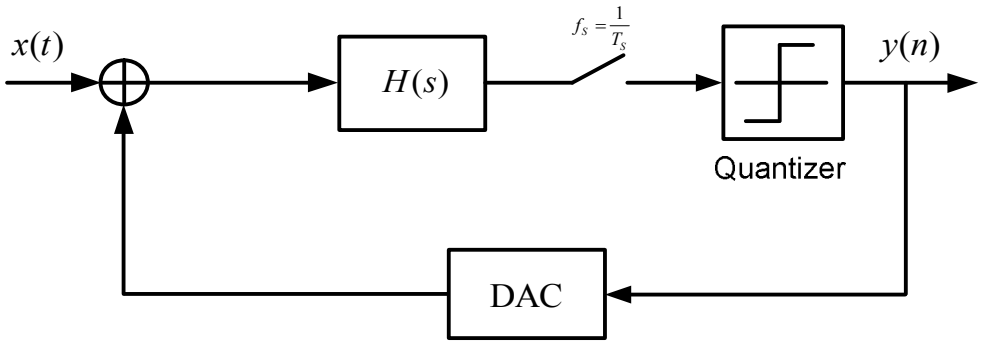


Figure 3.8 Typical 2nd-order CT bandpass ΣΔM

3.2 Resonator Model and Characteristic

Figure 3.8 shows a typical 2nd-order CT bandpass ΣΔM, where *H(s)* is the transfer function of the loop filter, usually a resonator. Although intuitively the loop filter can be directly replaced by the one port SAW/MEMS resonator, the straightforward replacement will not result in a functional bandpass ΣΔM. This is because (1) the one-port SAW/MEMS resonator does not have an ideal 2nd-order resonator transfer function, and (2) it is passive and has an insertion loss. These issues will be discussed in the following sub-sections.

3.2.1 Discussion of the Resonator Model

Figure 3.9 shows a model (dotted line) used for most of one-port SAW/MEMS resonators with a resistive load R_L, where R_m, C_m and L_m are the motional resistance, capacitance and inductance, respectively. C_p is the inherent static capacitance between the two terminals. Unlike in the ideal resonator whose transfer function is given in (3.1) in which the static capacitance, C_p does not exist,

$$H_{r,ideal}(s) = \frac{\frac{R_L}{L_m}s}{\left(s^2 + \frac{R_L + R_m}{L_m}s + \frac{1}{L_m C_m}\right)} = \frac{As}{\left(s^2 + \frac{\omega_0}{Q}s + \omega_0^2\right)} \tag{3.1}$$

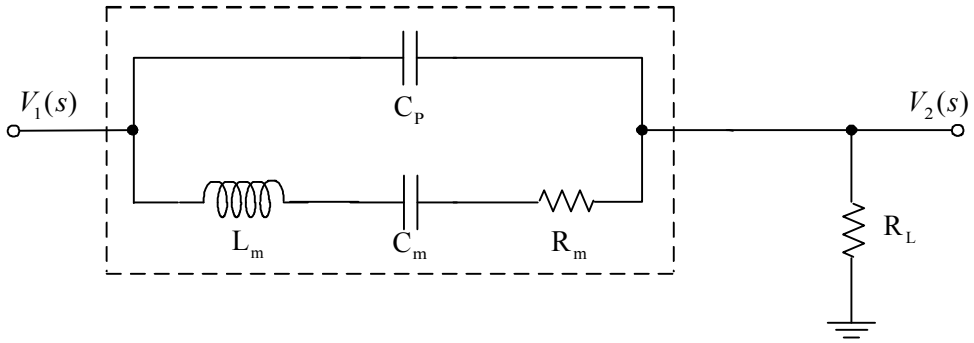


Figure 3.9 Model of one-port SAW/MEMS resonators.

where $\omega_0 = 1/\sqrt{L_m C_m}$ is the resonant frequency, $Q = \sqrt{L_m/C_m}/(R_L + R_m)$ and $A = R_L/L_m$, the transfer function of the practical one-port SAW/MEMS resonator in Figure 3-9 is given by

$$H_r(s) = \frac{V_2(s)}{V_1(s)} = \frac{s\left(s^2 + b_1 s + b_0\right)}{s^3 + a_2 s^2 + a_1 s + a_0} \tag{3.2}$$

where

$$a_0 = \frac{1}{L_m C_m R_L C_p},\ a_1 = \frac{(R_m + R_L)C_m + R_L C_p}{L_m C_m R_L C_p},$$

$$a_2 = \frac{R_m}{L_m} + \frac{1}{R_L C_p}, b_0 = \frac{C_p + C_m}{L_m C_m C_p} \text{ and } b_1 = \frac{R_m}{L_m}.$$

It is evident in (3.2) that there are pair of zeros at frequency $(b_0)^{1/2}$. Figure 3.10 shows the simulated frequency response of an SAW resonator with a resonant frequency of 47.3MHz (L_m = 84.12μH, R_m= 25Ω, C_m= 134.59fF, and C_p = 5pF) when the load resistance is 50Ω. The existence of the static capacitance, C_p, results in two modes of resonance, namely, series and parallel modes, whose corresponding frequencies are

$$\omega_0 = \frac{1}{\sqrt{L_m C_m}} \quad \text{and} \quad \omega_a = \frac{1}{\sqrt{L_m \dfrac{C_m C_p}{C_m + C_p}}}$$

respectively. This changes the ideal resonator transfer function, resulting in a notch (due to parallel resonance) just above the resonant frequency, referred to as “anti-resonance”.

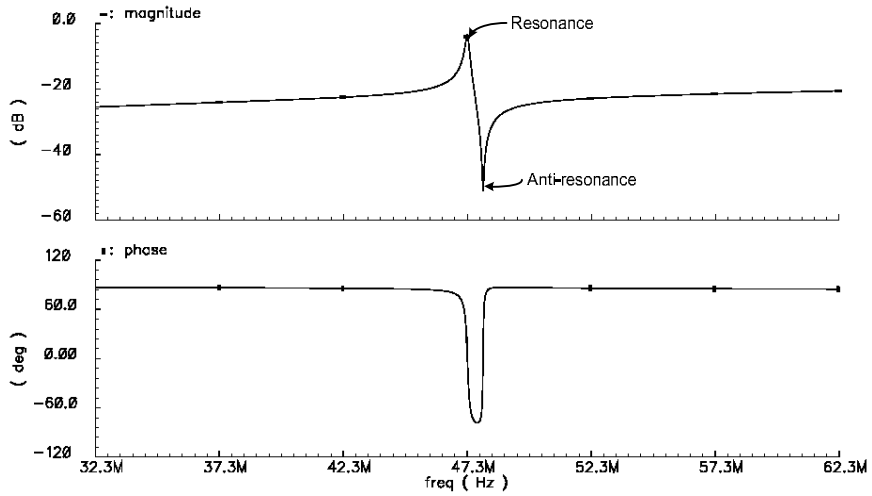


Figure 3.10 Simulated frequency response of a 47.3-MHz SAW resonator with a 50-Ω resistive load

The phase response is also altered. For the frequencies above the anti-resonance, the lagging phase becomes leading and the static capacitance effectively short-circuits the resonator.

Insertion loss (*IL*) of the SAW resonator results from the motion resistance R_m. According to (3.1), at resonant frequency, L_m and C_m cancel each other. The resonator becomes resistive. The insertion loss is therefore determined by R_m and R_L, that is

$$IL = \frac{R_L}{R_m + R_L} \tag{3.3}$$

Obviously, given a specific load R_L, the larger the motional resistance R_m, the larger the insertion loss. For the one-port SAW and MEMS resonators, the typical insertion losses are 1~15dB and 20~60dB, respectively. Note that the insertion loss is often measured with respect to a 50Ω load.

3.2.2 Anti-Resonance Cancellation

A simple method is proposed to cancel the effect of anti-resonance [106]. A capacitive path (C_c) is added and a differential signal is used to drive the resonator and

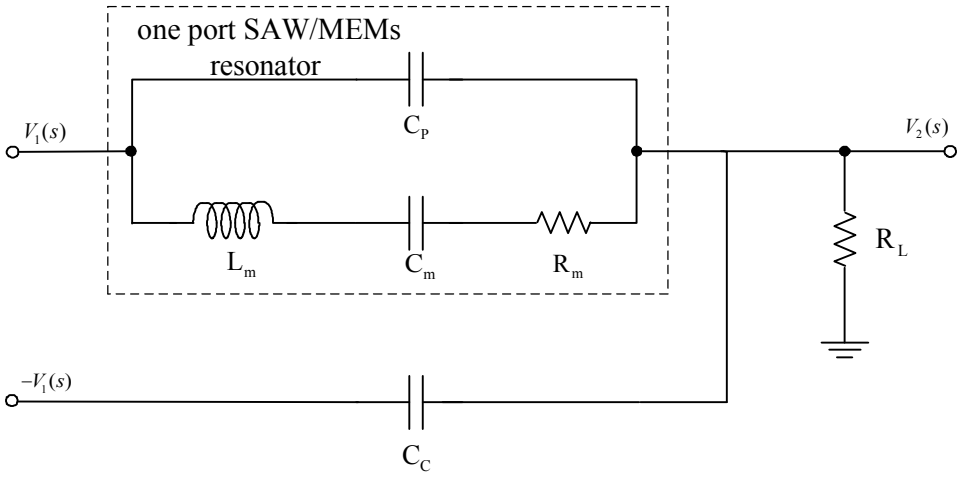


Figure 3.11 Anti-resonance cancellation circuit

C_c, as shown in Figure 3.11. The path C_c is effectively a negative capacitance. If C_c is made equal to C_p, the effect of C_p can be completely cancelled at the load. The resultant transfer function becomes

$$H_{r,cnl}(s) \approx \frac{\frac{R_L}{L_m}s}{\left(s^2 + \frac{R_L + R_m}{L_m}s + \frac{1}{L_m C_m}\right)\left(2R_L C_p s + 1\right)} \tag{3.4}$$

where $1/2R_LC_p >> R_L/L_m$, and $C_p=C_c$ are assumed. If $1/2R_LC_p$ is reasonably far away from the resonant frequency, $1/\sqrt{L_m C_m}$, the effect of the pole at $1/2R_LC_p$ can be ignored in the vicinity of the resonant frequency and (3.4) becomes

$$H_{r,cnl}(s) \approx \frac{\frac{R_L}{L_m}s}{\left(s^2 + \frac{R_L + R_m}{L_m}s + \frac{1}{L_m C_m}\right)} \tag{3.5}$$

which is same as the transfer function of the ideal resonator given by (3.1). Those assumption made for (3.4) and (3.5) are generally true for practical one-port SAW/MEMS resonators. Figure 3.12 shows the simulated frequency response of the SAW resonator with anti-resonance cancellation loaded with a 50-Ω resistor. It is

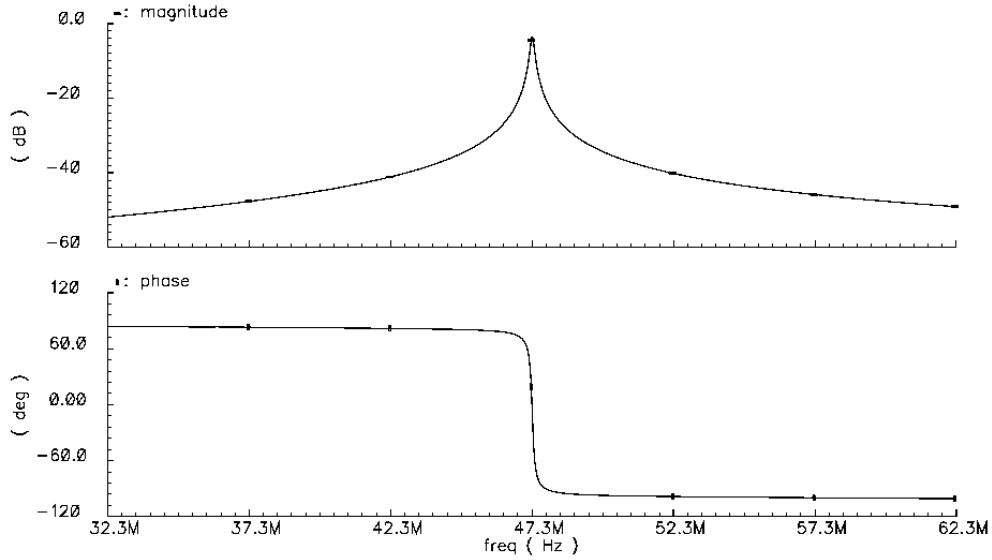


Figure 3.12 Simulated frequency response of a 47.3-MHz SAW resonator with anti-resonance cancellation

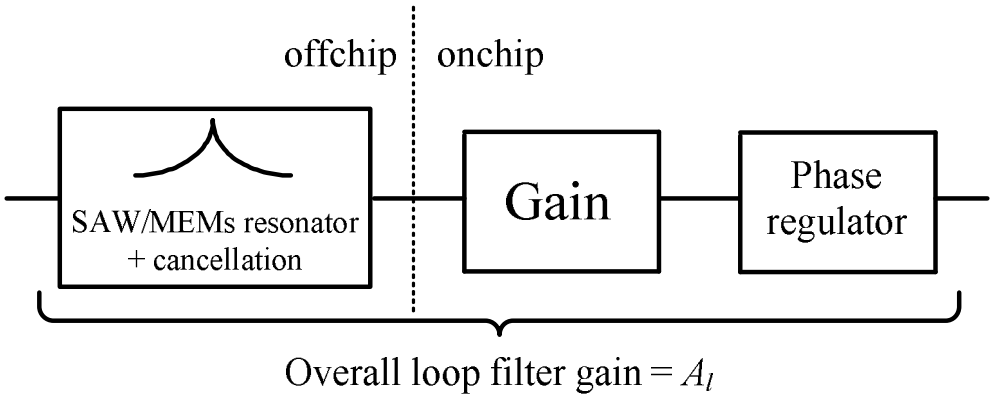


Figure 3.13 Block diagram of the proposed loop filter for the CT bandpass ΣΔM.

evident that the anti-resonance is removed. In the actual implementation, C_c is off chip and can be tuned to achieve the best cancellation.

3.2.3 Compensation of Insertion Loss

The insertion loss of the resonator can be easily compensated by adding a gain stage. However, such a gain stage inevitably introduces a phase delay in the forward path. Since the bandpass ΣΔM is a feedback system, any excess phase delay may deteriorate its performance and cause stability problem. To compensate the insertion loss without

introducing the excess phase delay, a gain stage with phase regulator is proposed. The phase regulator can be incorporated in the amplifier or be simply an allpass filter. Figure 3.13 depicts the block diagram of the proposed loop filter with anti-resonance cancellation and insertion loss compensation for CT bandpass ΣΔM. More detailed treatments of the insertion loss and phase compensation will be given in the next section.

It is also noted in (3.3) that the insertion loss depends on the load, R_L. Thus, the insertion loss can be reduced by simply increasing the load resistance. However, the large R_L may affect other parameters, such as the loaded Q of the resonator and the frequency response. As discussed in section 3.2.1, small R_L gives high Q, and reasonable high Q is needed in narrowband digitization. Thus, a trade-off is needed in choosing R_L. Figure 3.14 shows the Q and insertion loss vs. the load resistance for the 47.3-MHz SAW resonator used. For the OSR=473, resonator Q>100 is required to avoid significant SNR degradation in practical design. Therefore, R_L is chosen between 100 and 200 ohm with which insertion loss is less than 2dB, as indicated in Figure 3.14.

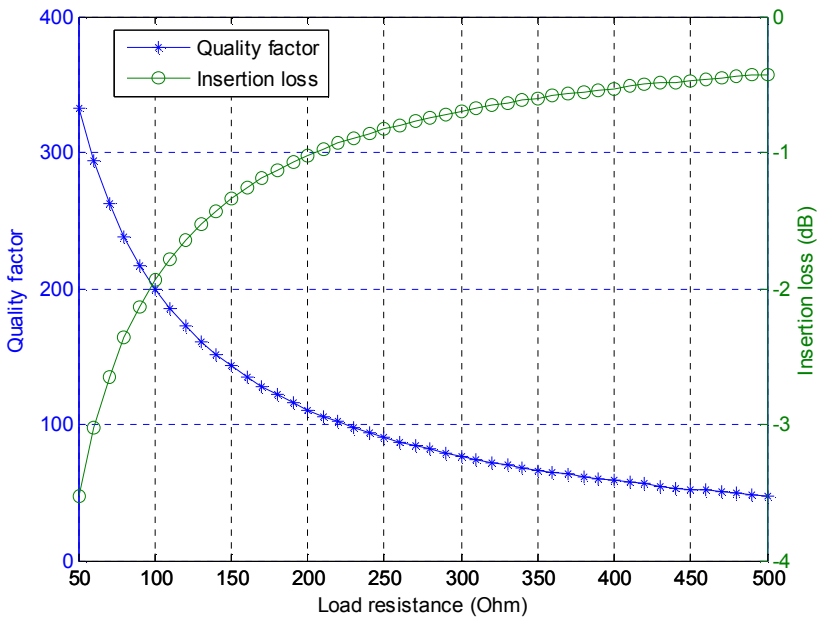


Figure 3.14 Resonator Q and insertion loss vs. load resistance

3.3 Bandpass ΣΔM Employing One-Port SAW/MEMS Resonators

In the integrators based CT bandpass ΣΔMs, only one DAC is used since the feedback/feedforward signals can be applied to the input of each integrator. Therefore, enough degree of freedom can be guaranteed to make it equivalent to the DT prototype. However, for the electromechanical resonator presented in last section, there is no internal node in the resonator can be accessed. To provide enough degree of freedom, several architectures have been proposed [30][50][107]. In this thesis, the architecture based on multi-feedback technique [107] is adopted.

3.3.1 Proposed Bandpass ΣΔM Architectures

The proposed 2nd-order bandpass ΣΔM employing one-port SAW/MEMS resonator as loop filter is shown in Figure 3.15 [106], in which multi-feedback technique is adopted. The details of the proposed loop filter have been discussed in the previous section and shown in Figure 3.13. Two feedback paths are formed by a return-to-zero (RZ), a half-return-to-zero (HRZ) DAC with two scaling factors, k_{RZ} and k_{HRZ}. A single bit quantizer is employed.

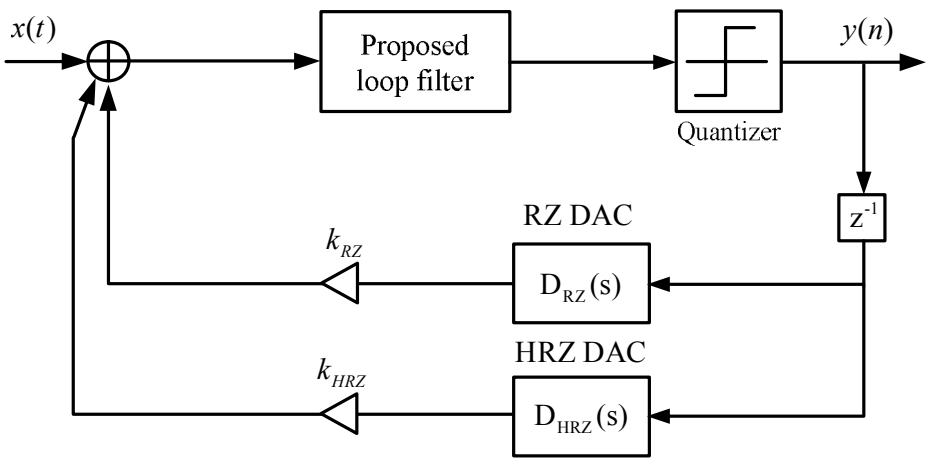


Figure 3.15 The proposed 2nd-order bandpass ΣΔM employing one-port SAW/MEMS resonator

The design of the CT bandpass ΣΔM follows the impulse-invariant transform where the loop transfer function from the output of the quantizer to its input should match between the CT and DT ΣΔM [108], that is,

$$H(z) = Z\{L^{-1}[H_{r,cnl}(s)D(s)]\Big|_{t=nT_s}\} \tag{3.6}$$

where T_s is the sampling period, $H(z)$ is the loop transfer function in DT domain, $H_{r,cnl}(s)$ is the transfer function of the resonator with anti-resonance cancellation and $D(s)$ is the linear combination of two DAC transfer functions,

$$D(s) = k_{RZ}D_{RZ}(s) + k_{HRZ}D_{HRZ}(s) \tag{3.7}$$

The transfer functions of the RZ and NRZ DACs are respectively given by

$$D_{RZ}(s) = \frac{1-e^{-sT/2}}{s} \quad and \quad D_{HRZ}(s) = \frac{e^{-sT/2}(1-e^{-sT/2})}{s} \tag{3.8}$$

For the 2nd-order modulator, the desired DT loop transfer function is

$$H(z) = \frac{z}{z^2+1} \tag{3.9}$$

Based on (3.6-3.9), the two scaling coefficients (k_{RZ} and k_{HRZ}) can be determined. The resultant coefficients are calculated by Matlab program as follows,

$$k_{RZ} = -1.1204 \quad and \quad k_{HRZ} = 2.6868 \tag{3.10}$$

Since the normalized resonator transfer function (normalized to the sampling frequency) is used in the above design, the coefficients can be virtually applied to the 2nd-order bandpass ΣΔMs with any center frequency that is a quarter of the sampling frequency.

A 4th-order bandpass ΣΔM is also proposed based on the same design methodology, as shown in Figure 3.16. The desired DT loop transfer function is

$$H(z) = \frac{2z^3+z}{(z^2+1)^2} \tag{3.11}$$

The resultant coefficients are

$$k_{RZ4} = -1.1262 \quad k_{HRZ4} = 2.7054 \quad k_{RZ2} = -1.0071 \quad k_{HRZ2} = 4.7022 \tag{3.12}$$

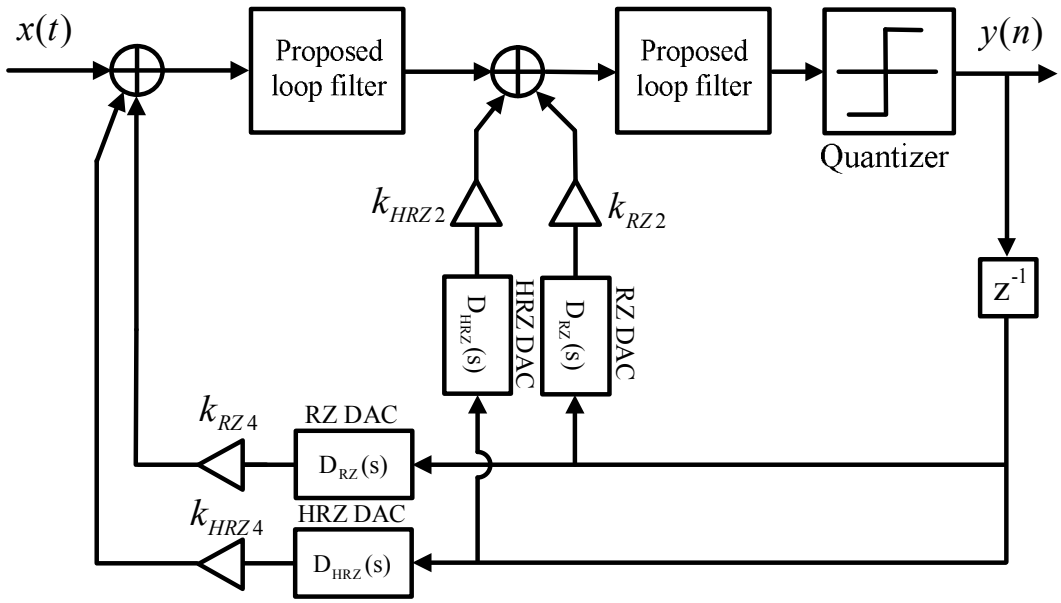


Figure 3.16 The proposed 4th-order bandpass ΣΔM employing one-port SAW/MEMS resonators

Since two resonators are needed for the 4th-order bandpass ΣΔM, mismatch of resonant frequencies between the two resonators may exist. In the case of practical one-port SAW/MEMS resonator, the tolerance of the resonant frequency is typically less than 0.1%. For the resonant frequency of 47.3MHz, the mismatch would be around several tens of kHz at the most. Simulation has shown that such a small frequency mismatch will not result in significant performance degradation in the proposed 4th-order bandpass ΣΔM. The simulated SNR degradation is less than 1.5dB.

3.3.2 Loop Filter Gain Determination

In general, a large gain in the forward path is required in bandpass ΣΔM to suppress the in-band quantization noise. The forward gain is determined by the gain of the loop filter (A_l) and that of the quantizer (A_q), as shown in a linear model in Figure 3.17. The gain of the one-bit quantizer is uncertain and depends on the magnitude of the input signal since the output of the quantizer is fixed. The smaller the input signal, the higher the quantizer gain. Thus, the gain of the loop filter has little effect on the overall forward

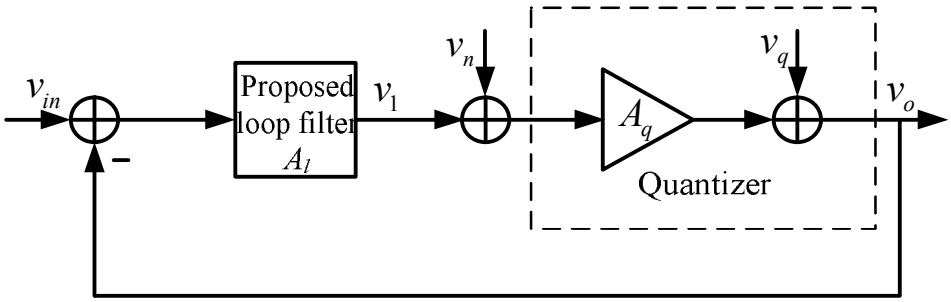


Figure 3.17 Simplified linear model of ΣΔM

gain, as long as it remains in the linear region and the quantizer has sufficient resolution. However, for low loop filter gain, the quantizer (comparator in the single-bit ΣΔM) has to work very hard to resolve the small output signal from the filter. This makes the overall modulator very sensitive to the non-idealities of the comparator, such as input offset, hysteresis and input referred noise. Assuming that all the comparator non-idealities and the thermal noise coming from the loop filter are modeled as an additive noise, v_n, injected at the input of the quantizer, the output of the modulator can be expressed as

$$\begin{aligned} v_o &= \frac{A_{fw}}{1+A_{fw}} v_{in} + \frac{1}{1+A_{fw}} v_q + \frac{A_q}{1+A_{fw}} v_n \\ &\approx v_{in} + \frac{1}{A_{fw}} v_q + \frac{1}{A_l} v_n \end{aligned} \tag{3.13}$$

where $A_{fw}>>1$ is assumed. Clearly, the quantization noise v_q is well attenuated by the large forward gain $A_{fw.}$, but v_n is only attenuated by A_l. If $A_l < 1$, v_n, is actually amplified, and hence deteriorates the SNDR of the modulator. Thus, the loop filter gain should be high enough to alleviate the problems caused by the quantizer (or comparator) non-idealities, but not too high to impose the burden on the gain stage, since wideband gain stage is difficult to design and consumes more power.

Figure 3.18 shows the simulated peak SNDR of the proposed 2nd-order bandpass ΣΔM employing SAW resonator with different loop filter gains at behavioral level

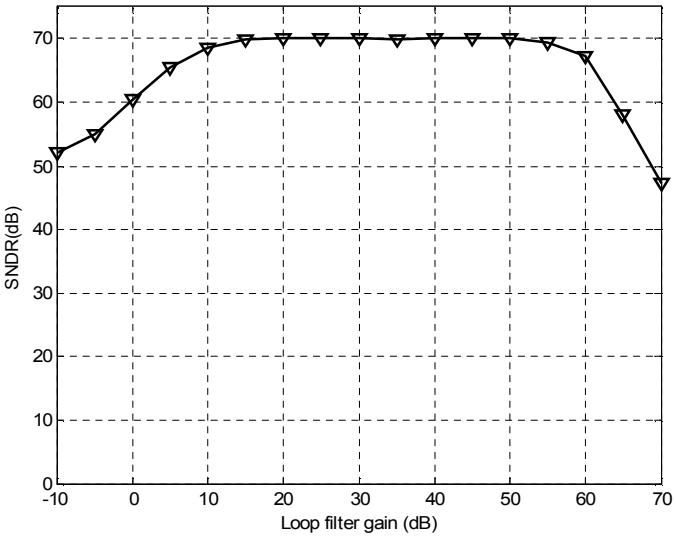


Figure 3.18 Simulated effect of loop filter gain A_l on SNDR performance in the 2nd-order bandpass ΣΔM

(Matlab). The peak SNDR is relatively unaffected for the loop filter gain between 15 to 55dB. However, it starts decreasing when the loop filter gain is beyond this range. The SNDR degradation at low loop filter gain reflects the effects of the non-ideal quantizer and the noise at its input, while the degradation at the high loop filter gain is due to the saturation of the loop filter output. The final loop filter gains are chosen to be externally adjustable from 15 to 40dB. For the 4th-order modulator, a similar process is used, assumed that two loop filters have equal gain in the simulation. The resultant loop filter gain is between 20 to 30dB for each loop filter (40 to 60dB in total).

3.3.3 Effect of Phase Delay in the Forward Path

To analyze the effect of phase delay, the gain stage is modeled by a first-order system with its transfer function being

$$A_G(s) = \frac{A_{G0}}{1 + s/\omega_p} \tag{3.14}$$

where A_{G0} is the DC gain and ω_p is the pole frequency. The phase delay (θ_d) introduced by the gain stage at the center frequency $\omega_{0,}$ is given by

$$\theta_d = \tan^{-1}\frac{\omega_0}{\omega_p} \tag{3.15}$$

Since this excess phase delay in the forward path effectively changes the transfer function, $H_{r,cnl}(s)$ in (3.5), the equivalence between the CT loop transfer function and its DT prototype $H(z)$ no longer exists. It is not difficult to understand that such an excess phase delay could deteriorate the SNR and may cause stability problem. To further prove it, the root locus plots of the noise transfer function for both 2nd- and 4th-order ΣΔM are obtained in Matlab and shown in Figure 3.19 and Figure 3.20 respectively, in which the phase delay θ_d is a parameter. The original NTFs without phase delay of the 2nd and 4th-order ΣΔMs are $1+z^{-2}$ and $(1+z^{-2})^2$, respectively. All poles of the NTF are located at the origin. It can be seen that as θ_d increases, the root loci move from origin towards the unit circle. The root loci approach unit circle at θ_d=90° in the 2nd-order case and at θ_d=34.4° for the 4th-order ΣΔM. This shows that the stability of the modulators worsen as phase

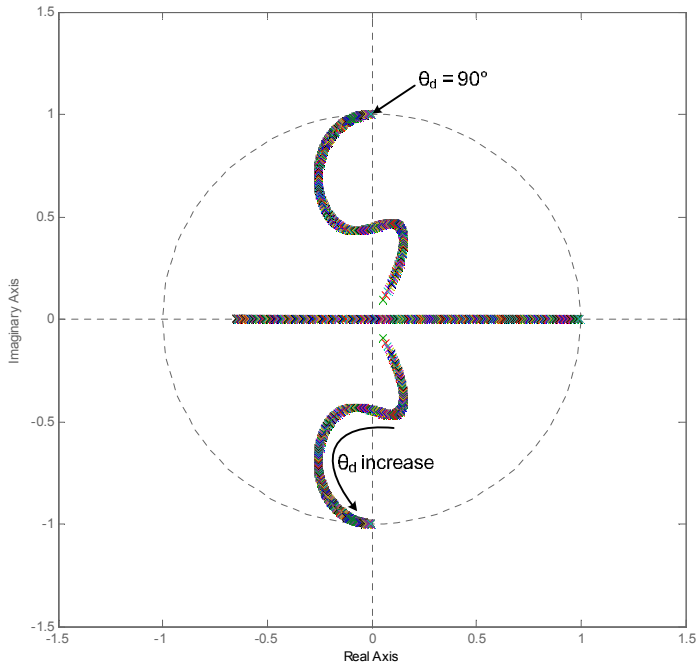


Figure 3.19 Root locus plots of the NTF for 2nd-order CT bandpass ΣΔM

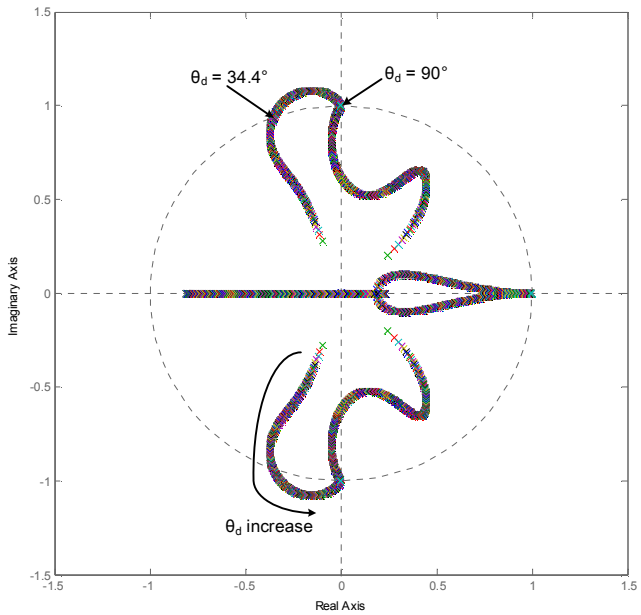


Figure 3.20 Root locus plots of the NTF for 4th-order CT bandpass ΣΔM

delay increases, especially for the higher-order ΣΔMs.

Since the root locus analysis does not give any information on performance degradation due to the phase delay in the forward path, a time-domain behavioral simulation (Matlab) is carried out to predict the SNR degradation. Figure 3.21 shows the result for the 2nd-order ΣΔM. The SNR degradation is within 3dB if the phase shift does not exceed ±15 degrees. However, the ΣΔM becomes unstable (oscillatory) when the overall phase shift is close to ±90 degrees, which is consistent with the result in Figure 3.19.

One way to compensate the phase delay is to adjust the feedback DAC coefficients as proposed in [109]. In practice, however, the DAC coefficient adjustment may be limited by the following factors. First, the DAC coefficients cannot be arbitrarily tuned since they are limited by the dynamic range at summing node. For example, if the DAC current (coefficient) is too large, the summing node could be saturated. Secondly, in

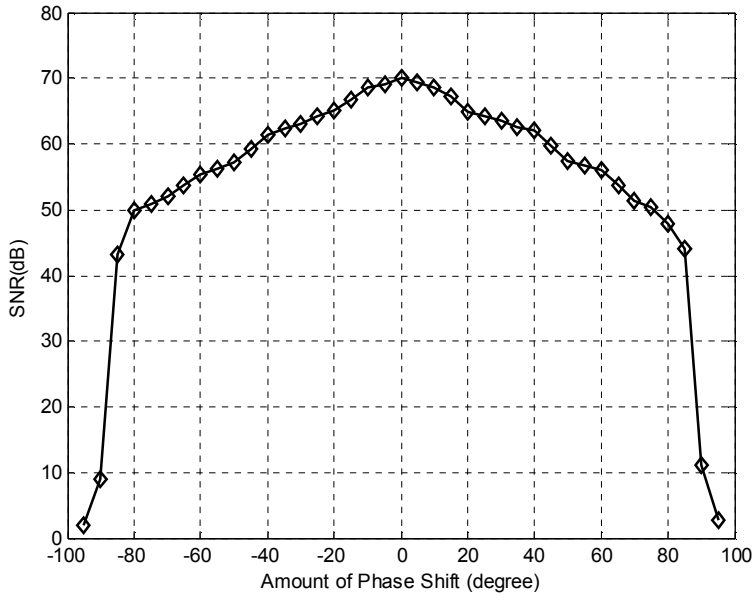


Figure 3.21 SNDR vs. phase shift in the 2nd-order CT bandpass SDM

[109], it shows that an excess phase delay of one sampling clock period can be fully compensated by tuning the feedback coefficients. However, it is achieved by assuming that there is physically no one clock period delay (implemented by hardware) embedded in the loop. Thus, with excess delay of one clock period, the equivalence between DT and CT can still be achieved by a new set of coefficients through tuning. In our design, however, one clock delay, introduced by two latches to reduce the metastability, already exists in the loop and hence the tuning of the DAC coefficients can only provide limited compensation to the excess phase delay. In other words, the exact match between the DT and CT transfer functions is no longer possible. Thirdly, in the case of higher-order modulator, multiple coefficients need to be tuned concurrently and thus it may be difficult to obtain the optimal value.

Our approach is to introduce a phase regulator in the forward path after the gain stage [106], as already shown in Figure 3.13. It can fully compensate the phase delay in the vicinity of the resonant frequency. The phase regulator can be an allpass filter, either

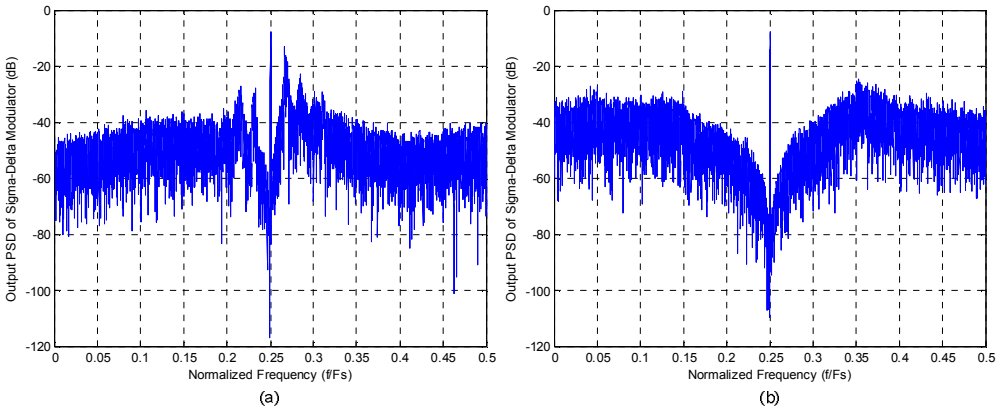


Figure 3.22 Simulated output spectrums (Matlab) of a 2nd-order CT BP ΣΔM without (a) and with (b) phase delay compensation

stand-alone or incorporated in the gain stage. In this paper, a tunable stand-alone allpass filter is adopted. Figure 3.22 shows the simulated output spectrums (Matlab) of a 2nd-order CT BP ΣΔM without (a) and with (b) allpass filter phase compensation. Clearly, the modulator without phase compensation is almost unstable and has poor SNR. The excess phase delay in the feedback path is minimized by circuit techniques which will be discussed in chapter 5.

3.4 Considerations of Non-Idealities in CT ΣΔM

While many kinds of non-idealities can limit the performances of CT bandpass ΣΔMs, they are particularly sensitive to some non-idealities associated with quantizer and feedback DACs, such as quantizer metastability, intersymbol interference, clock jitter and excess loop delay in feedback path. All these non-idealities will cause the error at the output of feedback DACs. As opposed to DT bandpass ΣΔMs, the value of the DAC output at any moment during a clock period is important in CT bandpass ΣΔMs. The DAC output is fed back directly to the input of the ΣΔM, and therefore input referred. Any error in the DAC output will appear at the output of the modulator and is not shaped by the loop filter.

3.4.1 Quantizer Metastability

For the single-bit ΣΔM, the quantizer is usually implemented with a comparator which uses a regenerative circuit. Ideally, the comparator will take a fixed amount of time to make a decision on its input. However, if the input of the comparator is too small, the regenerative circuit may not have enough time to resolve and cause metastability problem. Because the time when the input of comparator is close to zero (common mode voltage) is random, the effect of metastability can be modeled as a white noise which will degrade the dynamic range of the ΣΔM [109]. At very low input amplitudes, the ΣΔMs can even lock to some limit cycles, which prevents the ΣΔM from working properly [110].

The effect of metastability can be reduced by introducing additional latching stages after the comparator. In our designs, four cascade latches are used. The first latch acts as the one bit quantizer. The second latch, together with the third latch, provides one sampling period delay. The third and the fourth latch generate the control signal for the RZ and HRZ current-steering DACs, respectively. Since the signal needs to go through at least three latches before driving any DAC, the chance having metastability is greatly reduced. With the introducing of one sampling clock delay in the feedback loop, the loop transfer functions of the DT prototype ΣΔMs need to be modified as follows,

2^{nd}-order: $$H(z)\big|_{\text{no delay}} = \frac{z^{-2}}{1+z^{-2}} \rightarrow H(z)\big|_{\text{with delay}} = \frac{z^{-1}}{1+z^{-2}} = \frac{z}{z^2+1} \tag{3.16}$$

4^{th}-order: $$H(z)\big|_{\text{no delay}} = \frac{2z^{-2}+z^{-4}}{(1+z^{-2})^2} \rightarrow H(z)\big|_{\text{with delay}} = \frac{2z^{-1}+z^{-3}}{(1+z^{-2})^2} = \frac{2z^3+z}{(z^2+1)^2} \tag{3.17}$$

3.4.2 Intersymbol Interference

Non-zero and unequal rise/fall time in the DAC switching is one problem difficult to control by only circuit techniques. The resultant asymmetry between the positive and

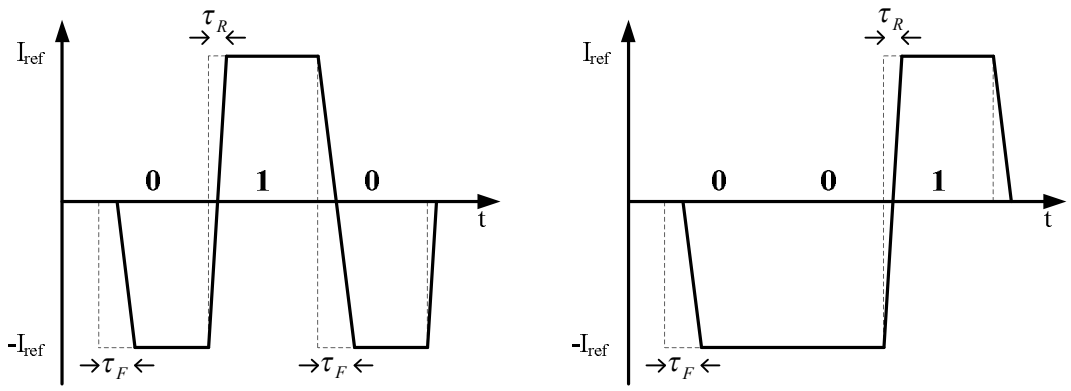


Figure 3.23 NRZ DAC waveform asymmetry for "010" and "001" bit sequence

negative DAC output waveforms will cause the intersymbol interference (ISI). They are almost inevitable in any practically DAC design. Figure 3.23 shows a NRZ DAC output with such ISI problem. Assuming that the rising edge is steeper than the falling edge ($\tau_R < \tau_F$), and the charge transfers during transition intervals τ_R and τ_F are not balanced out. Two bit sequences, 010 and 001, are used to analyze this problem. Clearly, the asymmetry of wave causes the energy contents (determined by charge delivered) of these two bit sequences different. Since the charge delivered with one symbol is not only dependent on the symbol itself but also on the previous symbol, this signal dependent imbalance can cause offset and introduce even-order harmonic distortion, hence reduce the SNDR performance of the CT ΣΔM [111].

Generally, there are three solutions to this ISI problem. The first and most straightforward one, is to design the DACs with short transition time and balanced transition edges. However, this may not be easy to realized, especially at high sampling frequencies. The second is to use differential instead of single-ended circuitry, in which the sum of two asymmetric single-ended DAC waveforms produces a symmetric differential DAC waveform [73][112]. Unfortunately, inherent single-ended SAW /MEMS filter is used as loop filter in this work. The circuitry can not be designed in fully-differential manner. The third, which is quite robust, is to apply RZ DACs, as

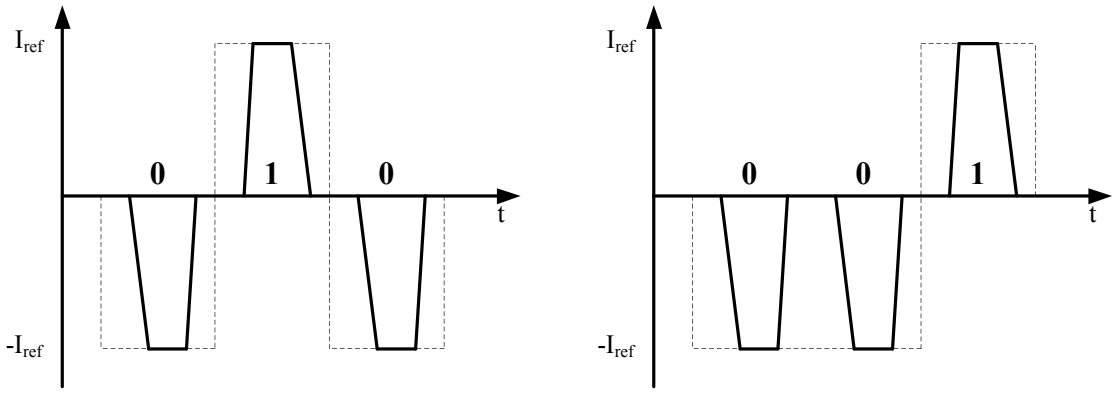


Figure 3.24 RZ DAC waveform asymmetry for "010" and "001" bit sequence

indicated in Figure 3.24. As a result, all DAC output pulses have a positive and a negative edge. The ISI problem is greatly reduced because, no matter how the previous DAC output, a new DAC output starts from the same reset value. In this work, RZ and HRZ DACs are employed to avoid the ISI problem.

3.4.3 Excess Loop Delay

The so-called excess loop delay [109] is a potential problem which only exists in CT ΣΔMs. Ideally, the DAC output should respond immediately to the quantizer clock edge. However, practical circuitry, including both comparator and feedback DACs, will introduce unwanted delays. The total time interval between the clock edge at the quantizer and the beginning of DAC output is referred to as excess loop delay, which is normally expressed as a fraction of the sampling period, $\tau_d = \rho_d T_S$, where $0 < \rho_d \leq 1$, as illustrated in Figure 3.25.

It can be shown that excess loop delay usually degrades the SNR performance of the ΣΔM and that for large delay, the ΣΔM can even become unstable [109]. As shown in Figure 3.26, only 20 % of the clock period delay has detrimentally increased the in-band noise floor of the output spectrum, and a peaking can be observed in the output spectrum which is due to the poles of NTF moving toward unit circle. Increasing the excess loop

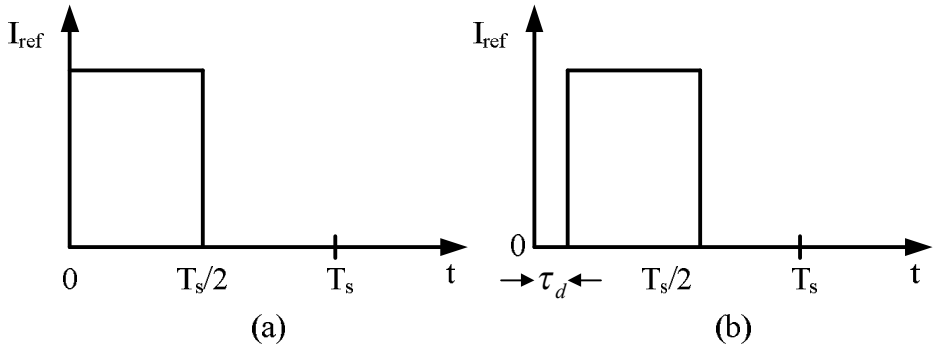


Figure 3.25 Illustration of the excess loop delay in RZ DAC

delay would enhance the peaking and eventually make the ΣΔM unstable. The notch also becomes narrow and shallow, which indicates the SNR degraded by the increased in-band noise.

Various methods have been proposed to compensate for the excess loop delay, such as adding extra feedback DAC branch or coefficient tuning of feedback DACs [51]. In this design, the effect of excess loop is carefully considered when determining the modulator structure. First of all, NRZ DAC, which is most sensitive to the excess loop delay, is avoided in the multi-feedback modulator structure. Secondly, as shown in Figure 3.27, the clock is routed opposite to the direction of signal propagation. In such a

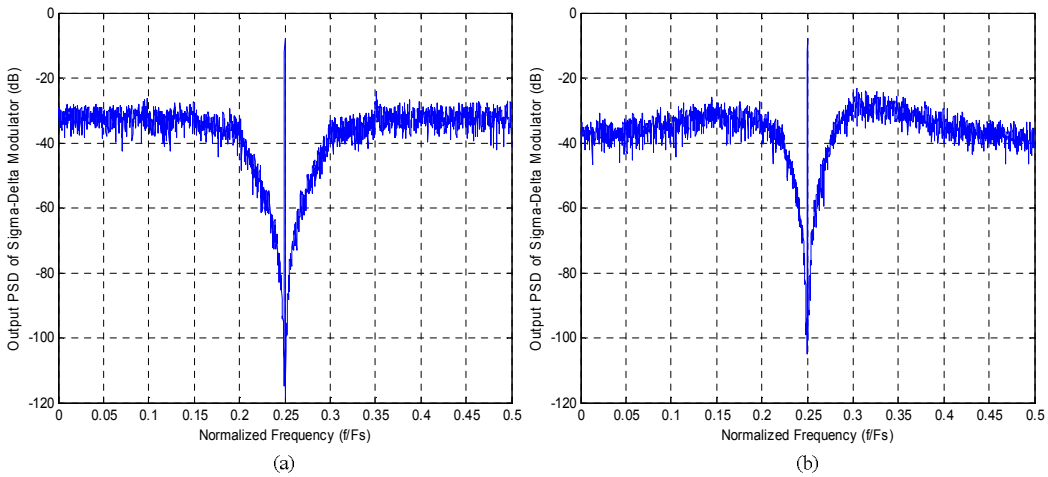


Figure 3.26 Behavioral simulations of a 4th-order CT bandpass ΣΔM (a) without excess loop delay and (b) with loop delay $\rho_d = 0.2$

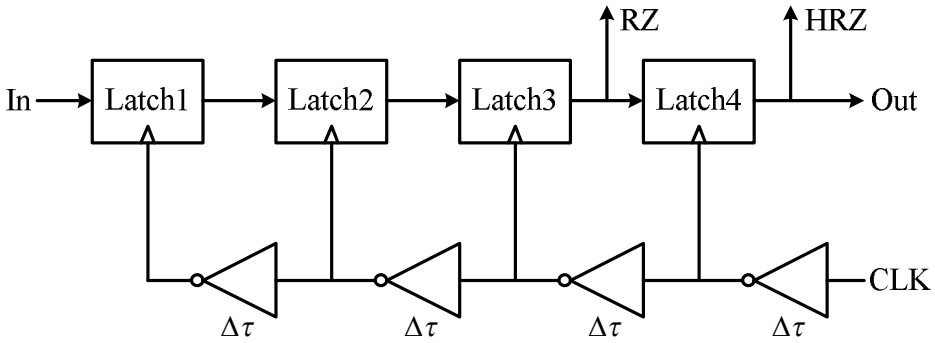


Figure 3.27 Clock configuration of 4 cascaded latches

way, the excess loop delay arising from the latches or quantizer and clock skew can be compensated. Furthermore, a programmable delayed inverter can be used, provide the possibility of tuning the excess loop delay compensation [113].

3.4.4 Clock Jitter Noise

In practice, the period of the clock signal presents random variations in its nominal values as shown in top of Figure 3.28. This is due to certain intrinsic uncertainties in the time in which clock transition occur, known as jitter. This clock jitter results in a non-uniform sampling which causes an increased noise power (appeared as a white noise) at the output of ΣΔMs [110].

The clock jitter degrades the SNR performance of both DT ΣΔMs and CT ΣΔMs and has been extensively studies in [110][114]. In DT ΣΔMs, the clock jitter effect mainly comes from the switched-capacitor amplifier (SCA) operation at the input of the ΣΔM. The output of the DAC in the feedback path is less susceptible to the clock jitter, since it is sampled at the end of the clock cycle where the signal is almost settled. In CT ΣΔMs, since there is no SCA at the input, the clock jitter mainly impacts on the DAC output.

In CT ΣΔMs with rectangle DACs' output waveforms indicated by Figure 3.28, the charge is transferred at a constant rate over a clock period, and so the charge transfer

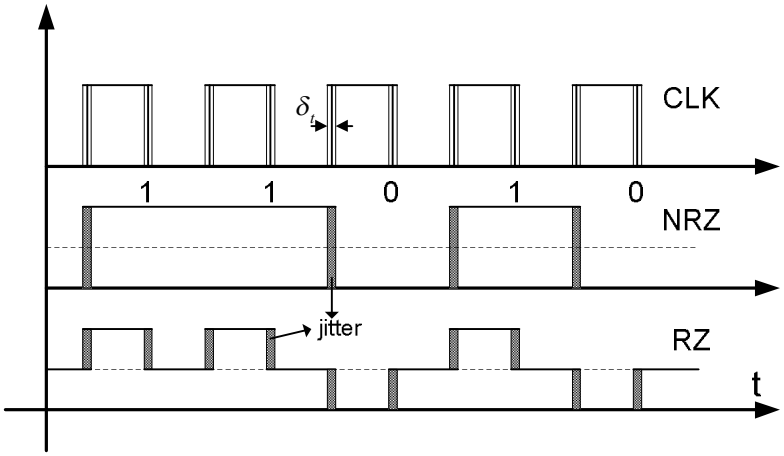


Figure 3.28 DAC waveforms in CT ΣΔMs with clock jitter for pattern "11010"

error is a large proportion of the total charge, therefore introduce more jitter noise. This jitter noise is directly added to the input signal, thus increasing the in-band noise power. The jitter noise power depends on the type of DAC. This is because jitter only matters when the DAC output changes sign. As illustrated in Figure 3.28, for the same bit sequence, the number of DAC output rising/falling edges per clock cycle will depend on the type of DAC. Intuitively, a lower SNR degradation can be achieved by using NRZ DACs, as Figure 3.28 predicts. The clock jitter will also introduce the error in the quantizer. However, similar to the quantization noise, the clock jitter noise in the quantizer is suppressed by the noise shaping and thus has less effect on the performance of the ΣΔM.

To understand the different sensitivities to clock jitter in DT and CT bandpass ΣΔMs, the analytical and simulated results given in [110][114] can be used to compare the SNR degradations. For the DT bandpass ΣΔM, the upper limit of the SNR due to jitter noise in the SCA operation can be estimated by

$$SNR_{\max}(dB) = 10 \cdot \log_{10} \frac{OSR^3}{\pi^2 \cdot \frac{\sigma_{DT,jitter}^2}{T_s^2}} \tag{3.18}$$

and that due to DAC's jitter noise in the CT bandpass ΣΔM is

$$SNR_{\max}(dB) = 10 \cdot \log_{10} \frac{OSR}{\alpha \cdot \frac{\sigma_{CT,jitter}^2}{T_s^2}} \tag{3.19}$$

where $\sigma_{DT,jitter}$ and $\sigma_{CT,jitter}$ are the standard deviations of the clock jitter in DT and CT ΣΔM, respectively, T_s is the sampling period, and α is a constant in the range of 4 to 48 depending on circuit architecture and the types of DACs used. To compare the jitter requirements for DT and CT ΣΔMs, (3.19) and (3.20) are set to be equal for same sampling frequency and OSR, yielding

$$\frac{\sigma_{CT,jitter}^2}{\sigma_{DT,jitter}^2} = \frac{\pi^2}{\alpha \cdot OSR^2} \tag{3.20}$$

Since normally, $OSR \geq 8$, $\alpha \geq 4$,

$$\frac{\sigma_{CT,jitter}^2}{\sigma_{DT,jitter}^2} \leq 0.0386 \tag{3.21}$$

this means that to achieve the same SNR, the clock jitter CT bandpass ΣΔM must be at least 30 times lower than that in the DT bandpass ΣΔM. In other word, the CT ΣΔM is more susceptible to the jitter noise.

Given OSR=473, α=48, $\sigma_{CT,jitter}$=2-ps (based on the maximum rms clock jitter of pulse generator used in the measurement) and T_s= 5.2854ns in our design, the peak SNR of the 4th-order bandpass ΣΔM is limited to 78.3dB according to (3.19). For the 2nd-order bandpass ΣΔM, the jitter specification can be relaxed to 20ps.

Some efforts have been made to overcome the jitter noise problem in CT ΣΔMs, which include the uses of multi-bit architecture, non-rectangle DAC shapes, and jitter noise averaging.

According to Figure 3.28, the jitter noise is proportional to the DAC step height. Each additional bit in the quantizer and in the DAC decreases the step height. Hence, the

jitter requirements can be relaxed [73][82][113], but at the cost of high circuit complexity and power consumption.

Another approach is to replace the conventional high jitter-sensitive rectangle DAC output waveform with low-jitter sensitive shape, which has the property of close-to-zero (common mode voltage) amplitude near the edge of clock signals so that clock variation in time has less effect compared with rectangle-shape DACs. A commonly used DAC is switched-capacitor DAC whose output waveform has an exponentially decaying shape [115-117]. An alternative solution, which can alleviate opamp speed requirements required by SC DACs, is to use sine-shaped DAC pulse [118]. However, it needs additional synchronization circuitry and introduces extra phase noise into the system.

The averaging method is to use finite response DAC (FIR DAC) in the feedback path [119][120]. With this DAC, the output pulse is widened over N clock and jitter noise is averaged over N periods. This approach can relax the jitter requirement quite efficiently at low to medium sampling clock with low power. A main drawback is that the analog FIR DAC introduces more loop delay which will deteriorate the modulator's stability, especially for high speed ΣΔMs.

The methods discussed above can help alleviate jitter problem in CT ΣΔMs, but only to some extent. A low-jitter or low phase-noise crystal/SAW oscillator for clock generation is still preferred to effectively reduce the jitter effects.

CHAPTER 4

CT BANDPASS ΣΔM BASED ON ELECTRO-MECHANICAL FILTER

The CT bandpass ΣΔMs presented in last chapter are only suitable for narrowband digitization since all the resonators have the same resonant frequency. For wideband applications, electromechanical filters with large bandwidth (>1MHz) may be good candidates. The advantages of using electromechanical filter as the loop filter are its wide range of available center frequencies and bandwidths, which can be customized to different applications. Furthermore, no frequency tuning is required. This chapter discusses the feasibility of electromechanical filter based bandpass ΣΔM. The concept is demonstrated in a 4^{th}-order SAW filter based CT bandpass ΣΔM with 110-MHz center frequency.

4.1 Candidate Electromechanical Filters

Electromechanical filters have different structures which result in different frequency responses or transfer functions. Not all the electromechanical filters can be used to realize bandpass ΣΔMs. In this section, some typical electromechanical filters are introduced and their suitability as loop filters in bandpass ΣΔMs is discussed.

4.1.1 SAW Filters

The SAW filters can be categorized in two major classes, namely, the transversal and the resonator-coupled filters. The transversal filters generally have wide passband or

high fractional bandwidth (5% to 50%). The fractional bandwidth is the ratio of 3-dB bandwidth of the filter over its center frequency, BW/f_c. The resonator-coupled filters, on the other hand, have much higher center frequencies up to several gigahertz, but much narrow passband or fractional bandwidth.

Transversal filter. A typical structure of the transversal filter is shown in Figure 4.1. It consists of two interdigital transducers (IDTs) on a piezoelectric substrate. The IDTs have two electrodes connected to source and load, respectively, so that a voltage applied to the left IDT causes electric fields in the gaps between the electrodes. The piezoelectric effect couples these fields to mechanical stresses which act as sources of SAWs, and the SAWs travel out of the transducer. At the output transducer on the right, the field associated with the incident wave induces voltages on the electrodes, which appears on the load at the output [98][99]. A SAW transversal filter is equivalent to a digital finite impulse response (FIR) filter in frequency response [98]. Therefore, a linear phase SAW transversal filter, which is desired in many wireless communication applications, can be easily implemented by designing the IDTs with *sinc* function pattern together with a proper window function used to suppress the passband ripples. Since the transfer function of the transversal filter is inherently a FIR filter, which means the transfer function of this filter contains only zeros, thus it is unsuitable for bandpass ΣΔMs.

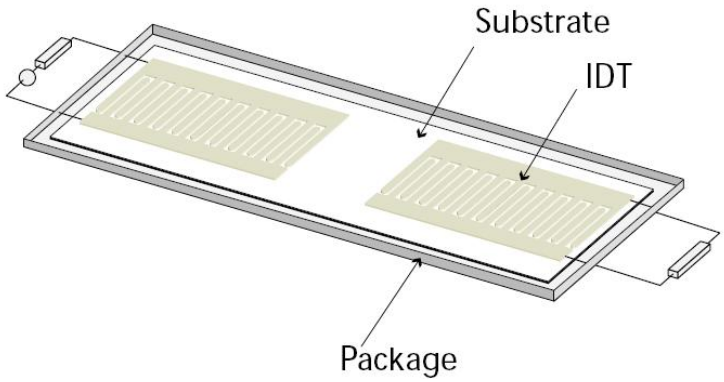


Figure 4.1 Transversal SAW filter

Resonator-coupled filter. The SAW filter can also be designed with proper coupled (connected) SAW resonators. In general, resonator-coupled SAW filters can be divided in to two categories, namely, the electrically- and the acoustically-(mechanically-)coupled filters. The electrically-coupled filter is also called impedance element filter (IEF) or ladder filter, which uses one-port SAW resonator as the basic element. There are several kinds of ladder filters, such as L type, T type, π type and lattice (bridge) type. The acoustically-coupled filters can be further divided into two categories, the transversely-coupled-resonators (TCRs) filter and the longitudinally-coupled-resonators (LCRs) filter.

Ladder filters offer low insertion loss and high power durability, compared with acoustically-coupled filters. L type ladder filter is a typical example, whose equivalent circuit is shown in Figure 4.2. In obtaining a bandpass response using the ladder elements (one-port SAW resonators) "1" and "2" shown in the dashed box in Figure 4.2, the aim is to adjust parameters so that the impedance Z_1 of "1" is minimized and the impedance Z_2 of "2" is maximized at center frequency f_c. This gives $f_{s1}=f_{p2}$, as sketched in Figure 4.3(a), where f_{s1} is the serial resonant frequency of resonator "1" and f_{p2} is the parallel resonant frequency of resonator "2". The desired bandpass transfer function $Z_2/(Z_1+Z_2)$ can be obtained, as shown in Figure 4.3(b). Obviously, this is a sixth-order bandpass response since the one-port SAW resonator has the order of three as indicated

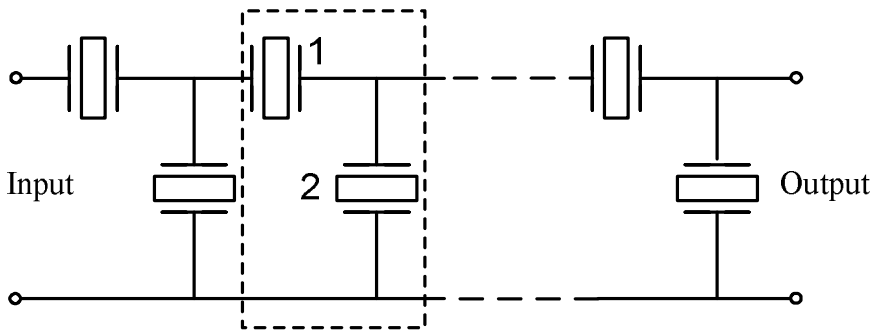
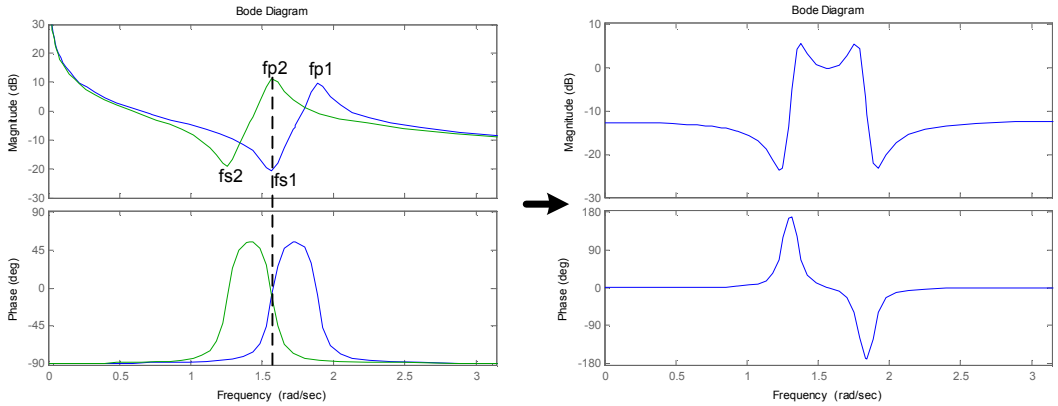


Figure 4.2 L type ladder filter



(a) (b)

Figure 4.4 Frequency response of (a) Z_1 and Z_2 and (b) $Z_2/(Z_1+ Z_2)$

by equation (3.2). The stopband rejection is quite poor, normally in the range of 10-20dB, if only one L-type element (one series resonator and one parallel resonator) is used. In practical SAW L-type ladder filter, to provide enough stopband rejection, 2~8 cascaded elements stages (4~16 resonators) are used to synthesize the filter. This results in a very high order (12~48) system, and makes the IEF filter not applicable for bandpass ΣΔM design.

A TCRs filter consists of two identical resonators fabricated close together, as shown in Figure 4.4, and relies on acoustic coupling between the two resonators. The equivalent circuit is given in Figure 4.5. The waves in one resonator extend slightly

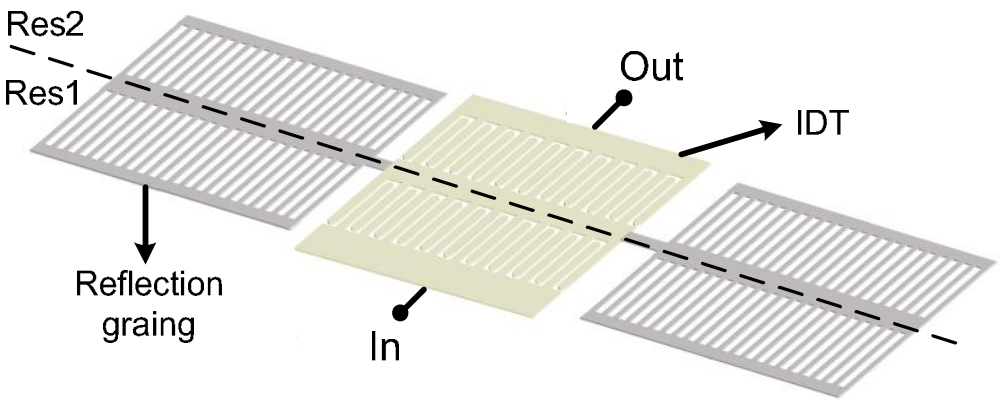


Figure 4.3 TCRs filter

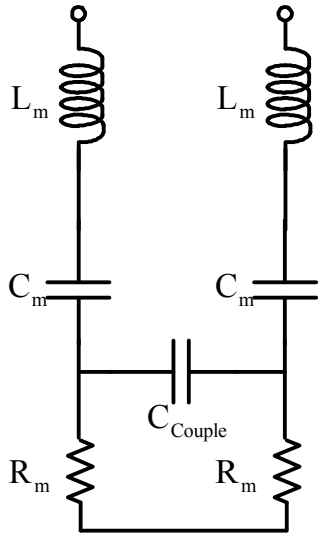


Figure 4.5 Equivalent circuit of TCRs SAW filter

outside its physical structure, and this enables some energy to leak from one resonator to the other. This couples the two resonators, and results in two pairs of conjugate poles. Because the input and output transducers are in different tracks, not facing each other, the stop band rejection can be good. It is common to cascade two devices to further improve the stopband rejection, and a rejection of around 50dB is obtainable. However, the use of resonances enables very narrow bandwidths to be obtained. In fact, this device is limited to fractional bandwidths below 0.2% (normally less than 200kHz) because the coupling between the two resonators is weak. Therefore, the TCRs SAW filter is not suitable for wideband bandpass ΣΔMs.

The LCRs filter is another type of acoustically-coupled SAW filter. A typical arrangement consists of two transducers in the space between two reflecting gratings. This is somewhat similar to the two-port resonator (as shown in Figure 3.3), but the two transducers are designed to resonate at two different frequencies. Using IDTs with strong internal reflections, the LCRs filter can be designed to have two pairs of high-Q conjugate poles (4^{th}-order transfer function). Fabricated on a strong-coupling substrate such as lithium tantalate or niobate, the LCRs filter can achieve insertion losses as low as

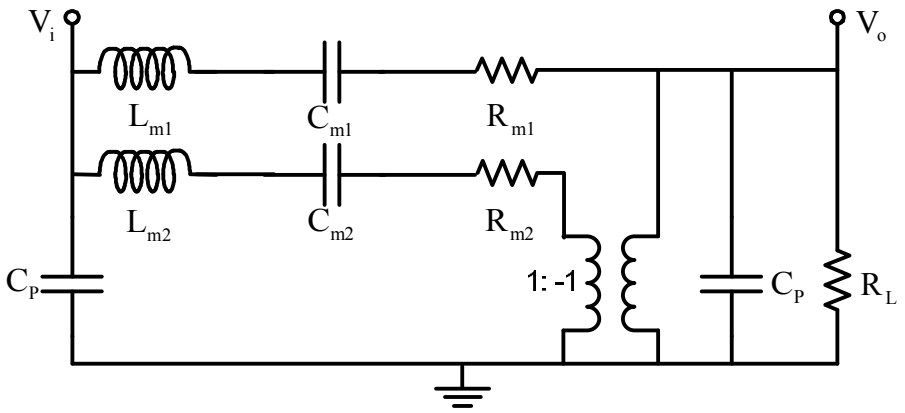


Figure 4.6 Equivalent circuit of LCRs SAW filter

2dB and stopband rejection as large as 70dB, at frequencies up to 2GHz. A fractional bandwidth up to 5% can be obtained for the LCRs filter without the need for tuning components. All the above properties make the LCRs filter very attractive to the wideband CT bandpass ΣΔM. The equivalent circuit of the LCRs filter is given in Figure 4.6. To derive the transfer function, the static capacitance C_p is temporally ignored to simplify the derivation. According to equivalent circuit, since

$$\begin{cases} Z_1 = R_{m1} + sL_{m1} + \dfrac{1}{sC_{m1}} & \omega_{c1}^2 = \dfrac{1}{L_{m1}C_{m1}} \\ Z_2 = R_{m2} + sL_{m2} + \dfrac{1}{sC_{m2}} & \omega_{c2}^2 = \dfrac{1}{L_{m2}C_{m2}} \end{cases} \tag{4.1}$$

the transfer function is given by

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{\dfrac{1}{Z_1} - \dfrac{1}{Z_2}}{\dfrac{1}{R_L} + \dfrac{1}{Z_1} + \dfrac{1}{Z_2}} = \frac{R_L(Z_2 - Z_1)}{Z_1Z_2 + R_L(Z_1 + Z_2)} \tag{4.2}$$

For the sake of simplicity, the motional resistances and inductances for the two resonators are assumed to be equal [98],

$$L_{m1} = L_{m2} = L_m \quad R_{m1} = R_{m2} = R_m \tag{4.3}$$

Therefore, (4.2) can be expanded to

$$H(s)=\frac{s\cdot\frac{R_L}{L_m}\left(\omega_{c2}^2-\omega_{c1}^2\right)}{\left(s^2+s\frac{R_L+R_m}{L_m}+\omega_{c1}^2\right)\cdot\left(s^2+s\frac{R_L+R_m}{L_m}+\omega_{c2}^2\right)-s^2\frac{R_L^2}{L_m^2}}$$
$$\approx\frac{s\cdot\frac{R_L}{L_m}\left(\omega_{c2}^2-\omega_{c1}^2\right)}{\left(s^2+s\frac{R_L+R_m}{L_m}+\omega_{c1}^2\right)\cdot\left(s^2+s\frac{R_L+R_m}{L_m}+\omega_{c2}^2\right)} \tag{4.4}$$

where ω_{c1} and ω_{c2} are generally chosen to be symmetric around a given center frequency ω_c, thus $\omega_c=(\omega_{c1}+\omega_{c2})/2$. Let $\omega_{c1}=\omega_c-\Delta\omega$ and $\omega_{c2}=\omega_c+\Delta\omega$, a good rule of thumb is to choose $2\Delta\omega=\omega_c/Q_r$, Q_r is the loaded quality factor of the constituent resonator, given by $Q_r=\sqrt{L_m/C_m}\big/\left(R_L+R_m\right)$ [99]. The resultant 3-dB filter bandwidth is BW=$4\Delta\omega$. The insertion loss around center frequency of this filter is determined by

$$IL=\left|H\left(j\omega_c\right)\right|\approx\frac{4\frac{R_L}{L_m}\Delta\omega}{\frac{R_m}{L_m}\cdot\frac{2R_L+R_m}{L_m}+4\left(\Delta\omega\right)^2} \tag{4.5}$$

Given a desired $\Delta\omega$, ($2\Delta\omega/\omega_c<1\%$) the load R_L need to be optimized to guarantee a low insertion loss less than 5dB. Together with the earlier discussions in section, the LCRs SAW filter may be a good candidate for the bandpass ΣΔM.

If C_p is included, the derivation of the transfer function is not trivial. A 6th-order transfer function will be obtained. However, if $1/R_LC_p$ is reasonably far away from the resonant frequencies and $1/R_LC_p >> R_L/L_m$, the 6th-order function can be simplified and well approximated by (4.5). These assumptions can be fulfilled by proper design of the interface circuits in the CT bandpass ΣΔMs which will be discussed later in section 4.3.1.

4.1.2 MEMS Filters

Commonly used MEMS filters include electrically- or mechanically-coupled micro-mechanic filters and thin film bulk acoustic wave resonator (FBAR) filters. In this thesis,

the vibrating MEMS filters which are comprised of properly coupled MEMS resonators [100][121] are of our interest. This kind of filters can achieve the merits of low insertion loss, high selectivity at very small volume. Owing to the electromechanical nature of the MEMS resonators, the coupling in vibrating MEMS filters can also be performed in either the electrical or mechanical domain, like in the SAW resonator-coupled filters.

In electrically-coupled MEMS filters, the coupling can be realized by passive (MEMS capacitor)/active (active buffers) elements [122], electrostatic force [123] and ladder connection similar to the SAW ladder filters [124][125][126]. Electrical coupling are suitable for realization of high-order bandpass filters. In the capacitive coupling filters, MEMS resonators are cascaded with a shunt capacitor connected to ground between every two adjacent resonators. This configuration results in several resonance modes in the system and consequently the bandpass frequency response [122]. Another approach used for implementation of high-order MEMS filter is to electrically cascade MEMS resonators using active buffers or amplifiers. With the aid of these active components, the loading effect can be eliminated to some extent. Thus the multiplication of resonators' transfer functions results in an overall high-order system with several pairs of conjugate poles [122]. Electrostatic force between two closely-spaced MEMS resonator can also be used to construct high-order coupled resonators bandpass filters. No additional physical coupling elements are needed [123]. The above three approaches (capacitive, active and electrostatic coupling) have been used to realize MEMS filters with very impressive frequency characteristics, such as low IL and good stopband suppression, but only at relatively-low center frequency (less than 1MHz). On the other hand, ladder type MEMS filters are capable of operating at much higher frequencies up to 800MHz [126], but have relatively-low stopband rejection. This makes ladder type MEMS filters not suitable for bandpass ΣΔMs design.

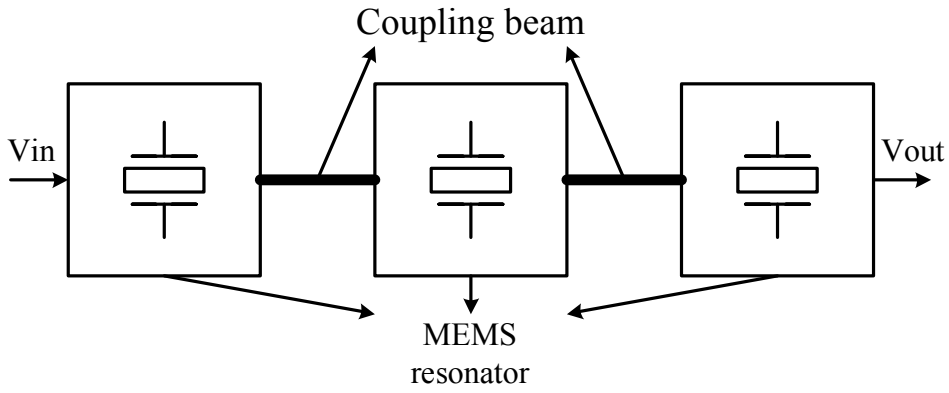


Figure 4.7 Mechanically-coupled MEMS filter

A mechanical system with *n* degree of freedom has *n* resonant modes. Therefore, if a number of MEMS resonators are cascaded mechanically with vibrating coupling beams, as shown in Figure 4-7, the resulting structure will be a bandpass filter with multiple resonances. Several mechanically-coupled filters, most of which use polysilicon or SOI micromachining technology, have been realized with different types of MEMS resonators such as CC-beam resonator[100][127], disk resonator [125], coupled-array composite resonator[128], and combination of disk resonator and wine glass ring resonator [129]. This kind of MEMS filters can be realized with center frequencies as high as 800MHz [126], stopband rejections as large as 50dB [129], and fractional bandwidths up to 1%. A typical equivalent circuit of 2-resonator mechanically-coupled MEMS filter is shown in Figure 4-8. According to KCL and KVL, we have

$$\begin{cases} V_1 = I_o \cdot \left(Z_2 - \dfrac{1}{sC_B} + R_L \right) \\ \dfrac{V_i - V_1}{Z_1 - \dfrac{1}{sC_B} + R_s} = I_o + \dfrac{V_1}{\dfrac{1}{sC_B}} \\ V_o = I_o \cdot R_L \end{cases} \tag{4.6}$$

and with

$$Z_1 = R_{m1} + sL_{m1} + \frac{1}{sC_{m1}} \quad \text{and} \quad Z_2 = R_{m2} + sL_{m2} + \frac{1}{sC_{m2}} \tag{4.7}$$

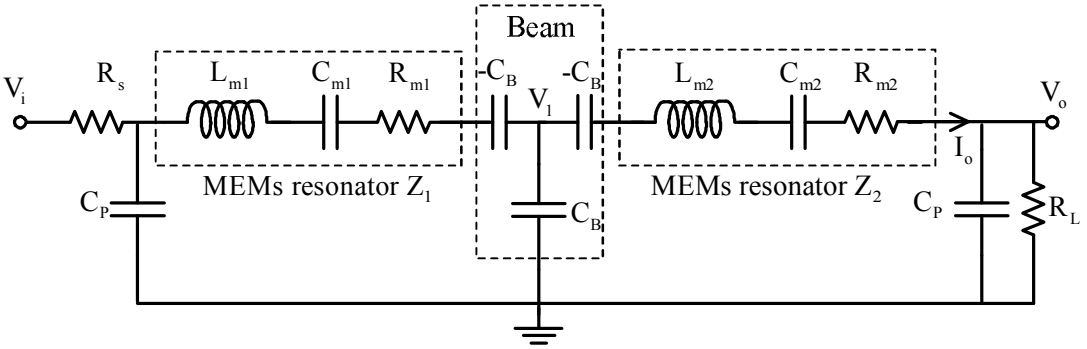


Figure 4.8 Equivalent circuit of 2-resonator mechanically-coupled MEMS filter

the filter transfer function is given by

$$H(s)=\frac{V_o(s)}{V_i(s)}=\frac{R_L\cdot\dfrac{1}{sC_B}}{\left(Z_1+R_s+\dfrac{1}{sC_B}\right)\left(Z_2+R_L-\dfrac{1}{sC_B}\right)+\left[\left(Z_1-Z_2\right)+\left(R_s-R_L\right)\right]\cdot\dfrac{1}{sC_B}} \quad (4.8)$$

In most of the mechanically-coupled MEMS filters, two identical resonators are adopted and R_s and R_L can be chosen to be equal, that is

$$Z_1=Z_2=Z=R_m+sL_m+\frac{1}{sC_m} \quad \text{and} \quad R_s=R_L \quad (4.9)$$

This will further simplify (4.8) to

$$H(s)=\frac{R_L\cdot\dfrac{1}{sC_B}}{\left(Z+R_L-\dfrac{1}{sC_B}\right)\left(Z+R_L+\dfrac{1}{sC_B}\right)} \quad (4.10)$$

After re-arranging,

$$\begin{aligned} H(s)=\frac{V_o(s)}{V_i(s)} &= \frac{s\cdot\dfrac{R_L}{C_BL_m^2}}{\left(s^2+s\dfrac{R_L+R_m}{L_m}+\dfrac{1}{L_mC_m}\dfrac{C_B-C_m}{C_B}\right)\left(s^2+s\dfrac{R_L+R_m}{L_m}+\dfrac{1}{L_mC_m}\dfrac{C_B+C_m}{C_B}\right)} \\ &= \frac{s\cdot\dfrac{R_L}{2L_m}\left(\omega_{c2}^2-\omega_{c1}^2\right)}{\left(s^2+s\dfrac{R_L+R_m}{L_m}+\omega_{c1}^2\right)\cdot\left(s^2+s\dfrac{R_L+R_m}{L_m}+\omega_{c2}^2\right)} \end{aligned} \quad (4.11)$$

in which

$$\begin{cases} \omega_c^2 = \dfrac{1}{L_m C_m} \\ \omega_{c1}^2 = \omega_c^2\left(1-\dfrac{C_m}{C_B}\right) \Rightarrow \omega_{c1} = \omega_c\sqrt{1-\dfrac{C_m}{C_B}} \approx \omega_c\left(1-\dfrac{C_m}{2C_B}\right) = \omega_c - \Delta\omega \\ \omega_{c2}^2 = \omega_c^2\left(1+\dfrac{C_m}{C_B}\right) \Rightarrow \omega_{c2} = \omega_c\sqrt{1+\dfrac{C_m}{C_B}} \approx \omega_c\left(1+\dfrac{C_m}{2C_B}\right) = \omega_c + \Delta\omega \\ \Delta\omega = \omega_c \dfrac{C_m}{2C_B} \end{cases} \tag{4.12}$$

It can be seen that (4.11) almost shares the same form of (4.4), except that numerator is divided by two. Therefore, the mechanically-coupled MEMS filters may also be used as the loop filters for CT bandpass ΣΔMs. Similarly, if $2\Delta\omega=\omega_c/Q_r$, Q_r is the loaded Q factor of the constituent resonator, given by $Q_r = \sqrt{L_m/C_m}\big/\left(R_L + R_m\right)$, the coupling beam should be designed with

$$C_B = Q_r \cdot C_m \tag{4.13}$$

The resultant 3-dB filter bandwidth is BW=$4\Delta\omega$. The insertion loss around center frequency of this filter is determined by

$$IL = \left|H\left(j\omega_c\right)\right| \approx \frac{2\dfrac{R_L}{L_m}\Delta\omega}{\left(\dfrac{R_L+R_m}{L_m}\right)^2 + 4\left(\Delta\omega\right)^2} \tag{4.14}$$

Given a desired $\Delta\omega$, ($2\Delta\omega/\omega_c$<1%) the load R_L need to be optimized to guarantee a low insertion loss less than 5dB.

In summary, the LCRs SAW filter and the mechanically-coupled MEMS filter appear to be suitable candidates for realization of CT bandpass ΣΔMs. Their transfer function in (4.4) and (4.11) can be generalized to

$$H(s) = \frac{As}{\left(s^2 + \dfrac{\omega_c}{Q_r}s + \omega_{c1}^2\right)\cdot\left(s^2 + \dfrac{\omega_c}{Q_r}s + \omega_{c2}^2\right)} \tag{4.15}$$

4.2 Bandpass ΣΔMs Employing Electromechanical Filters

As the transfer functions of the candidate electromechanical filters in (4.15) is almost fixed and there is no internal node which can be used to synthesize the desired loop filter for the CT bandpass ΣΔMs, multi-feedback structure is used to provide required controllability and obtain the desired loop transfer function that matches the optimized DT prototype modulator. A LCRs SAW filter with center frequency f_c=110MHz and 3-dB bandwidth BW=4Δf=1.152MHz is used to design the electromechanical filter based CT bandpass ΣΔM.

4.2.1 DT Prototype Determination

The 4th-order DT loop filter defined by (3.11) or (3.17) in last chapter places all the NTF zeros (poles of loop filter) at the same frequency (f_s/4, $z = \pm j$), because two identical resonators are used. For wideband ΣΔMs, the SNR can be significantly improved by spreading the NTF zeros across the signal band, especially for the wideband ΣΔMs with low to moderate oversampling ratios. Generally, these NTF zeros can be placed around the $z = \pm j$ on the unit circle. Moreover, the complex poles of the NTF are needed to be located within the unit circle surrounding the signal band to ensure a stable modulator. This is more important for higher order ΣΔMs (order ≥ 4). In general, Lee's rule and extensive simulations are used to optimize the locations of the NTF's poles.

A straightforward estimate for the optimal placement of the NTF zeros of a bandpass ΣΔM with signal band center at f_S/4 can be calculated by minimizing

$$\int_{\frac{f_s}{4}-\frac{f_B}{2}}^{\frac{f_s}{4}+\frac{f_B}{2}} 2\left|\prod_{l=1}^{L}\left(z+e^{j\pi/2+2\pi f_l}\right)\left(z-e^{j\pi/2+2\pi f_l}\right)\right|^2 df \quad \text{with} \quad z=e^{j2\pi f} \tag{4.16}$$

where $2L$ is the order of the bandpass ΣΔM, and $(\pm j\pi/2)+2\pi f_l$ (l=1…L) are the normalized angular frequencies of the NTF zeros. To simply the analysis, the expression for the lowpass ΣΔM after the transformation of $z^2 \to -z$ is used, which is given by

$$\int_0^{f_B} 2\left|\prod_{l=1}^{L}\left(z-e^{2\pi f_l}\right)\right|^2 df \quad \text{with} \quad z=e^{j2\pi f} \tag{4.17}$$

and $2\pi f_l$ are now the normalized angular frequencies. In order to have a loop filter with real valued coefficients, complex zeros should occur in conjugated pairs. For a 2nd-order lowpass modulator (equivalent to a 4th-order bandpass modulator), its NTF zeros should be placed at $z=e^{\pm j2\pi\alpha}$. The frequency α can be determined by calculating

$$\min_{\alpha}\int_0^{f_B} 2\left|\left(z-e^{j2\pi\alpha}\right)\left(z-e^{-j2\pi\alpha}\right)\right|^2 df \quad \text{with} \quad z=e^{j2\pi f} \tag{4.18}$$

This is equivalent to calculate

$$\min_{\alpha} 2\left[4\pi f_B\left(2+\cos(4\pi\alpha)\right)+\sin(4\pi f_B)-8\sin(2\pi f_B)\cos(2\pi\alpha)\right] \tag{4.19}$$

The solution to this optimization problem can be obtained by differentiating (4.19) with respect to α, and equating the result to zero. Therefore, the optimal solution for the NTF zeros placement can be solved as,

$$\alpha=\cos^{-1}\left(\frac{\sin 2\pi f_B}{2\pi f_B}\right)\xrightarrow{f_B\ll 1}\approx\frac{\sqrt{3}}{3}f_B \tag{4.20}$$

After the lowpass to bandpass transformation, the optimal NTF zeros for the 4th-order bandpass ΣΔM is given by

$$z=e^{j((\pm\pi/2)\pm 2\pi(\alpha/2))}=e^{j\left((\pm\pi/2)\pm\frac{\sqrt{3}}{3}\pi f_B\right)} \tag{4.21}$$

The optimal spreading of the NTF zeros of the 4th-order bandpass ΣΔM increases the SNR with approximately 3.5dB [85] compared with placing all the zeros at $z=\pm j$. Note that the optimization process above assumed that the quantization noise is white, and that the poles of the NTF have no significant effect on the in-band noise. A more

accurate optimization may take into account the effects for NTF poles and dependency of quantization on input signals, etc. Nevertheless, the optimal zeros for a 4^{th}-order modulator given in (4.21) are good enough for a practical design purpose.

The in-band quantization noise is reduced as the distance of the poles from the origin of the unit circle increases. However, at the same time, this increased distance results in an increase in the NTF magnitude at out-of-band frequencies far from the center frequency. Consequently, the total quantization noise power increases, thus the modulator becomes prone to instability. Therefore, a number of constraints must be considered when to determine the poles of the NTF. First of all, the overall noise transfer function *NTF(z)* must be realizable, which means *NTF(∞)*=1. Secondly, as the out-of-band NTF magnitude and hence the stability of the ΣΔM is largely determined by the choice of NTF poles, the positions of the poles should be designed to guarantee the modulator's stability. Lee's rule is adopted in this design because of its simple form and good reliability. At last, since the STF and NTF of the modulator structure in this chapter have the same poles, they need to be placed to achieve flat magnitude response over the signal band.

For the 110-MHz LCRs SAW filter with $BW=4\Delta f$=1.152MHz, the pole frequencies of this SAW filer have already been determined by $f_c \pm \Delta f$ =110±0.288MHz, and loaded Q of constituent resonator is $Q_r = f_c/2\Delta f$=191. Its simulated frequency response based on the equivalent circuit given in Figure 4.6 is shown in Figure 4.9. Note that the static capacitances C_p is ignored here. According to (4.21), in which $\alpha=2\Delta f=BW/2$, DT bandpass prototype loop filter with such poles placements can achieve an optimal SNR performance in a signal bandwidth of $f_B=\sqrt{3}\alpha=\sqrt{3}BW/2$=1MHz. After normalization, the pole frequencies (zero frequencies of the NTF) in z-domain is given by

$$z = e^{j((\pm\pi/2)\pm 0.00411263)} \tag{4.22}$$

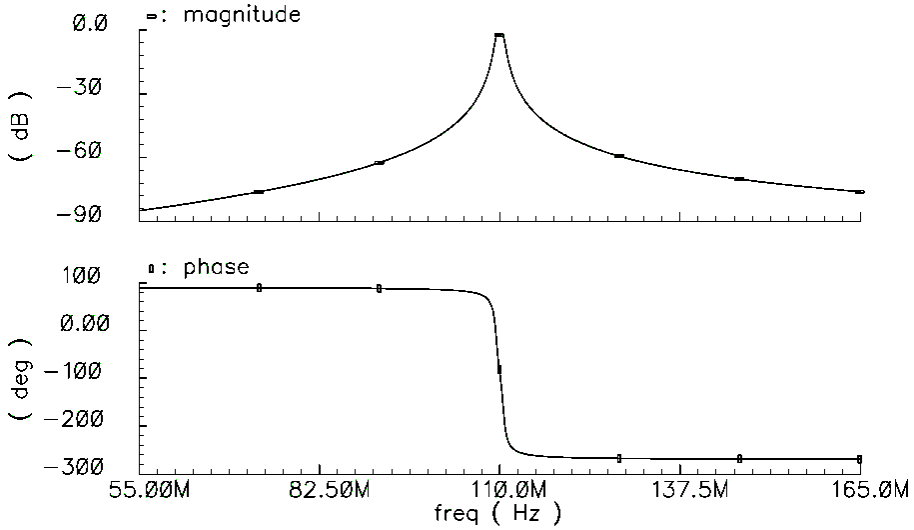


Figure 4.9 Simulated frequency response of a 110-MHz LCRs SAW filter

Thus, the numerator of the designed NTF is given by

$$num_{NTF} = z^4 + 1.999932z^2 + 1 \tag{4.23}$$

instead of z^4+2z^2+1 where there is no zeros spreading. To ensure stability and achieve good SNR at the same time, instead of putting all the poles of NTF at origin, they are optimally placed by an iteration process based on Lee's rule. A Matlab program is written to perform all above consideration and the resultant NTF is given below

$$NTF(z) = \frac{z^4 + 1.999932z^2 + 1}{z^4 + 0.763907z^2 + 0.236059} \tag{4.24}$$

in which NTF magnitude limit in Lee's rule is set to be 2. Note that there are no odd powers of z in the NTF transfer function due to the symmetry of the poles and zeros about the imaginary axis of the z-plane, which is a direct consequence of centering the conversion signal band at $f_s/4$. The simulated frequency response of this NTF is shown in Figure 4.10. The corresponding transfer function of the loop filter is

$$H(z) = \frac{1 - NTF(z)}{NTF(z)} = \frac{1.236025z^2 + 0.763941}{z^2 + 1.999932z^2 + 1} \tag{4.25}$$

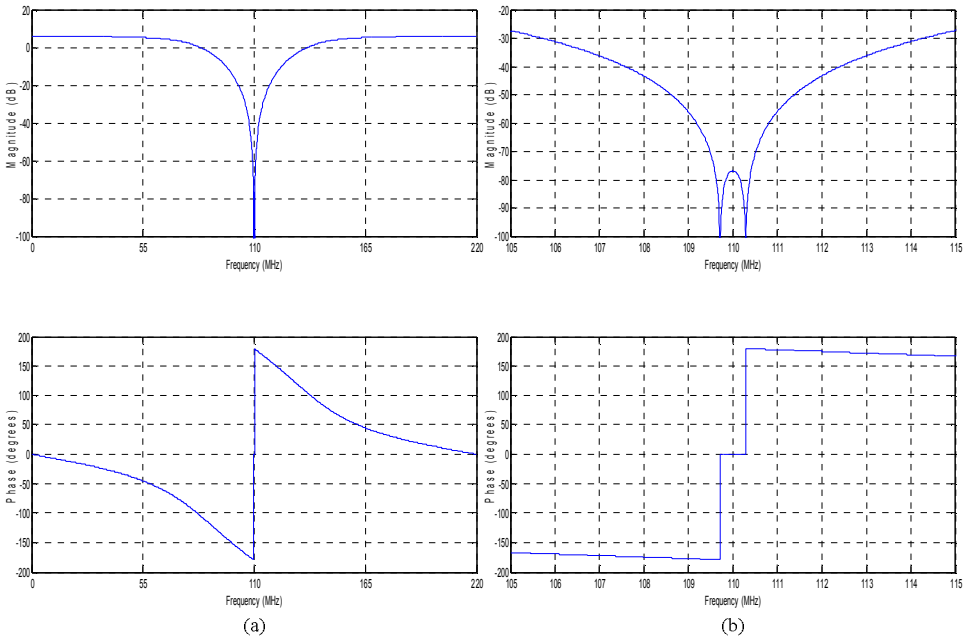


Figure 4.10 (a) Simulated response of the designed NTF and (b) its zoomed-in view

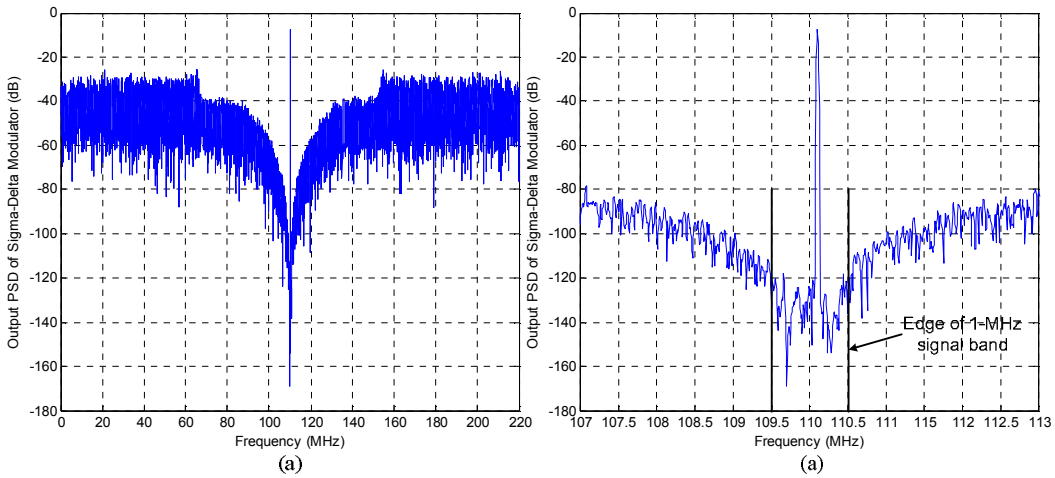


Figure 4.11 (a) Simulated output spectrum of the designed DT bandpass ΣΔM and (b) its zoomed-in view

This transfer function is used to construct a DT prototype bandpass ΣΔM at behavioral level. A time-domain simulation is done in Matlab and the output spectrum of this ΣΔM is shown in Figure 4.11. Two notches caused by the NTF zeros are clearly visible in the signal band. SNR of 98dB can be achieved in a 1-MHz signal band, where poles of loop filter (zeros of NTF) have ideal infinite Q.

4.2.2 Equivalence between CT and DT ΣΔMs

Due to the lack of the internal nodes of the LCRs SAW filter, multi-feedback structure is applied to obtain the equivalent loop transfer function between CT bandpass ΣΔM and the DT prototype, according to the impulse-invariant transform given in (3.6) , which is rewritten,

$$H(z) = Z\{L^{-1}[H(s)D(s)]\Big|_{t=nT_s}\} \tag{4.26}$$

in which *H(z)* is given in (4.25), *H(s)* is in (4.15), *D(s)* is the linear combination of feedback DAC transfer functions. To realize the equivalence, the sampling period T_s is normalized to 1 and Q_r is assumed to be ideally infinite, thus *H(s)* is simplified to

$$H(s) = \frac{A's}{\left[s^2 + \left(\frac{\pi}{2} + \pi\alpha\right)^2\right] \cdot \left[s^2 + \left(\frac{\pi}{2} - \pi\alpha\right)^2\right]} \tag{4.27}$$

where α=0.0013091 for the given LCRs SAW filter. Intuitively, four independent tunable DACs are needed to obtain the equivalence. RZ and HRZ DACs are used to reduce the intersymbol interference as discussed in last chapter. Considering that one sampling period delay is needed right after the quantizer to compensate the metastability problem, the resultant ΣΔM structure is shown in Figure 4.12. The equivalence can be expressed as

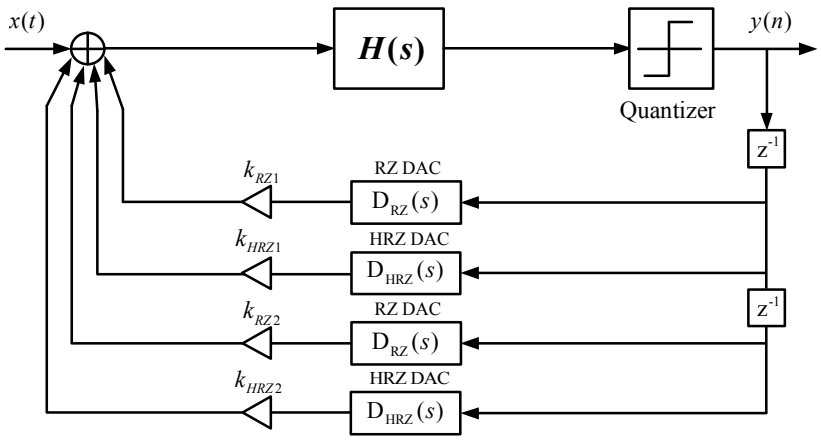


Figure 4.12 CT bandpass ΣΔM with loop filter H(s)

$$H(z) = k_{RZ1}z^{-1}H_{RZ}(z) + k_{HRZ1}z^{-1}H_{HRZ}(z) + k_{RZ2}z^{-2}H_{RZ}(z) + k_{HRZ2}z^{-2}H_{HRZ}(z) \quad (4.28)$$

or after rearranging,

$$z^2H(z) = k_{RZ1}zH_{RZ}(z) + k_{HRZ1}zH_{HRZ}(z) + k_{RZ2}H_{RZ}(z) + k_{HRZ2}H_{HRZ}(z) \quad (4.29)$$

in which

$$\begin{aligned} H_{RZ}(z) &= Z\{L^{-1}[H(s)D_{RZ}(s)]\big|_{t=nT_s}\} \\ &= \frac{0.109430z^3 + 0.099128z^2 - 0.177149z - 0.019576}{z^4 + 1.999932z^2 + 1} \end{aligned} \quad (4.30)$$

and

$$\begin{aligned} H_{HRZ}(z) &= Z\{L^{-1}[H(s)D_{HRZ}(s)]\big|_{t=nT_s}\} \\ &= \frac{0.019576z^3 + 0.177149z^2 - 0.099128z - 0.109430}{z^4 + 1.999932z^2 + 1} \end{aligned} \quad (4.31)$$

,respectively. According to the *H(z)* in (4.25), the left side of (4.29) has 5 numerator coefficients (4^{th}-order numerator), but there are only 4 tunable parameters on the right side. To provide full controllability, one more NRZ DAC with its output fed back to the input of quantizer is added, as shown in Figure 4.13. Thus, five feedback coefficients can be determined by

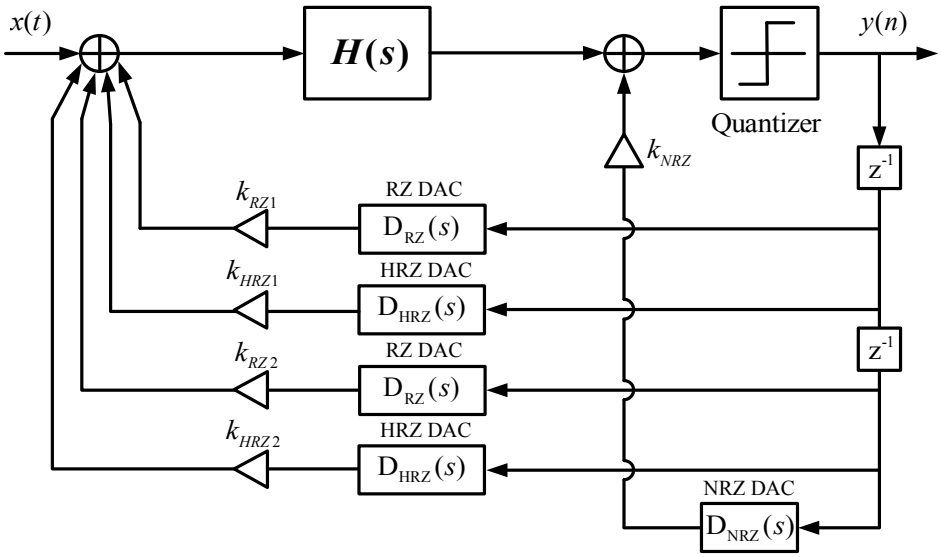


Figure 4.13 Modified CT bandpass ΣΔM with loop filter H(s)

$$\begin{aligned} H(z) = {} & k_{RZ1}z^{-1}H_{RZ}(z) + k_{HRZ1}z^{-1}H_{HRZ}(z) \\ & + k_{RZ2}z^{-2}H_{RZ}(z) + k_{HRZ2}z^{-2}H_{HRZ}(z) \\ & + k_{NRZ}z^{-2}H_{NRZ}(z) \end{aligned} \tag{4.32}$$

, yielding

$$\begin{cases} k_{RZ1} = 7.703716 \\ k_{HRZ1} = -4.410976 \\ k_{RZ2} = -0.642040 \\ k_{HRZ2} = 4.495381 \\ k_{NRZ} = 0.479360A' \end{cases} \tag{4.33}$$

in which

$$H_{NRZ}(z) = \frac{z^4 + 1.999932z^2 + 1}{z^4 + 1.999932z^2 + 1} = 1 \tag{4.34}$$

The simulated output spectrum of the designed CT bandpass ΣΔM is shown in Figure 4.14. It is very close to the simulation result of the DT prototype given in Figure 4.11, and the SNR performance in 1-MHz signal bandwidth is almost the same. Therefore, the equivalence is well established. So far, the quality factor Q_r of the constituent resonator is assumed to be infinite during the derivation. In practice, the effect of Q_r must be included to predict the performance of modulator more accurately. For the given

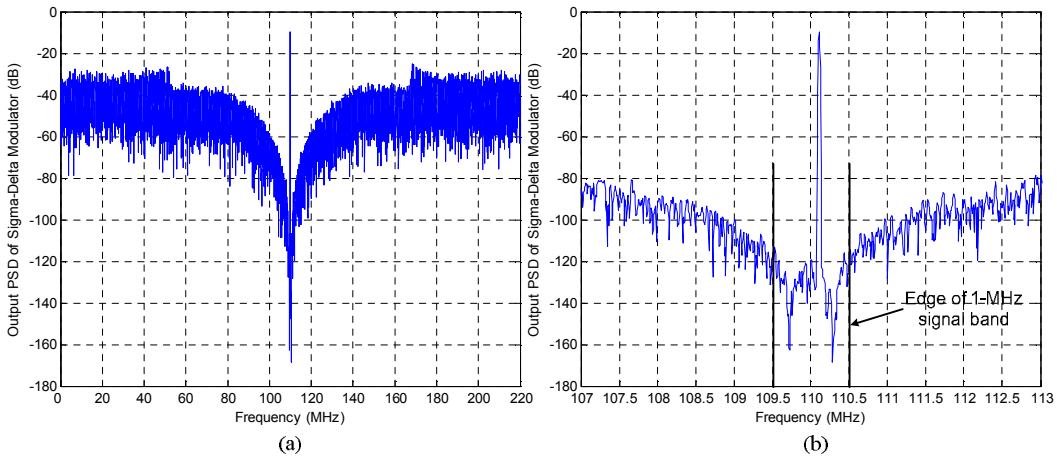


Figure 4.14 (a) Simulated output spectrum of the designed CT bandpass ΣΔM and (b) its zoomed-in view

practical LCRs SAW filter, the estimated Q_r is 191, the filter transfer function $H(s)$ given in (4.27) needs to be modified to

$$H(s)=\frac{A's}{\left[s^2+\frac{\pi/2}{Q_r}s+\left(\frac{\pi}{2}+\pi\alpha\right)^2\right]\cdot\left[s^2+\frac{\pi/2}{Q_r}s+\left(\frac{\pi}{2}-\pi\alpha\right)^2\right]} \tag{4.35}$$

The re-calculated feedback coefficients are

$$\begin{cases} k_{RZ1} &= 7.709969 \\ k_{HRZ1} &= -4.316128 \\ k_{RZ2} &= -0.770370 \\ k_{HRZ2} &= 4.580499 \\ k_{NRZ} &= 0.480415A' \end{cases} \tag{4.36}$$

From the simulation result shown in Figure 4.15, the NTF zeros are not as clear as that in Figure 4.14 and the SNR performance in 1-MHz degrades by about 6-dB. The feedback coefficients given in (4.36) have six decimal places, which are undesirable in practical design. After the coefficients are truncated to be with only 2 decimal places, the SNR degradation is less than 1dB, which is good enough for practical design.

The above equivalence assumes that the transfer function of the LCRs SAW filter has the form of (4.15) or (4.27). For the practical filter, the motional resistances and

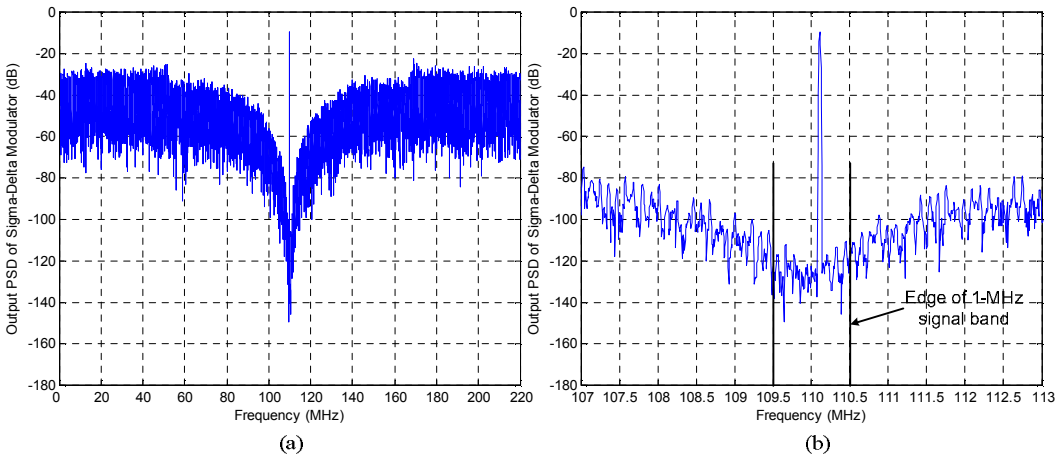


Figure 4.15 (a) Simulated output spectrum of the designed CT bandpass ΣΔM with Q=191 and (b) its zoomed-in view

inductances of the constituent resonators may not be ideally equal. Consequently, a more general form of the transfer function given below may be used, which is

$$H_1(s) = \frac{As^3 + Bs^2 + Cs + D}{\left(s^2 + \frac{\omega_c}{Q_r}s + \omega_{c1}^2\right)\cdot\left(s^2 + \frac{\omega_c}{Q_r}s + \omega_{c2}^2\right)} \tag{4.37}$$

$H_{RZ}(z)$ and $H_{HRZ}(z)$ employing $H_1(s)$ have the same denominators as those in (4.30) and (4.31). Even though the numerators are different, the highest order is 3. Therefore, the equivalence between CT and DT ΣΔMs can still be achieved by re-calculating the feedback coefficients as long as the exact transfer function of the LCRs SAW filter is known.

Although the design example in this sub-section is for a 4th-order a LCRs SAW filter based bandpass ΣΔM, the design methodology proposed here can be extended to the mechanically-coupled MEMS filter based CT bandpass ΣΔMs since they have the same transfer function.

4.3 Non-Idealities Considerations

Ideally, the methodology presented in last section can be used to design CT bandpass ΣΔMs employing LCRs SAW filters or mechanically-coupled MEMS filters with superior performance, as long as their transfer functions having the form of (4.15). However, some non-idealities will greatly compromise the performance of the resultant ΣΔMs or even make them unfunctional. Therefore, these non-ideal effects must be carefully studied.

4.3.1 Non-Idealities in the Filters

Among the non-idealities of the LCRs SAW filter and the MEMS mechanically-coupled filter, the inherent insertion loss and the static capacitance associated with input and output terminals are of major concern.

The effect of insertion loss on the performance of modulator has been well studied in section 3.2.3 and 3.3.2. In general, a wideband gain stage is needed to compensate this loss and alleviate the stringent requirement on the quantizer. Typical insertion loss for the two interested electromechanical filters is in the range from 1.5dB to 10dB. Therefore, for one-bit quantizer, similar to the electromechanical resonator based ΣΔM, an extensive circuit-level simulation is also needed to determine the minimal required forward loop gain. For the 4^{th}-order ΣΔM described in the last section, 50-dB gain is needed before the output signals of the LCRs SAW filter are quantized. This gain is provided by the gain stage (30dB) after the LCRs SAW filter and the pre-amplifier (20dB) of the quantizer.

In section 4.1, the static capacitance C_p associated with the input/output terminals of the filters is ignored in the derivations of the filter transfer functions. This static capacitance includes not only the capacitance from filter structure itself, but also the capacitances from bonding pad and PCB since the electromechanical filter is connected externally in the practical implementation. The MEMS filter has small physical size, its static capacitance is only in range of several tens of femto-farads, and therefore can be ignored. This implies that, if the MEMS filter can be integrated with the electronic circuitry on the same substrate, its transfer function will match closely that in (4.15). This is a very desirable property. The LCRs SAW filter, on the other hand, generally has large static capacitance (2 to 4pF) because of its large physical size. Together with the parasitic capacitance in the pad and PCB, the externally connected LCRs SAW filter will have an equivalent static capacitance 5 to 8pF at its input/output port. This capacitance will limit the bandwidth of the gain stage after electromechanical filter.

For the ΣΔM employing 110-MHz LCRs SAW filter, this limited bandwidth caused by the parasitic capacitance will introduce a quite large phase delay in the forward path

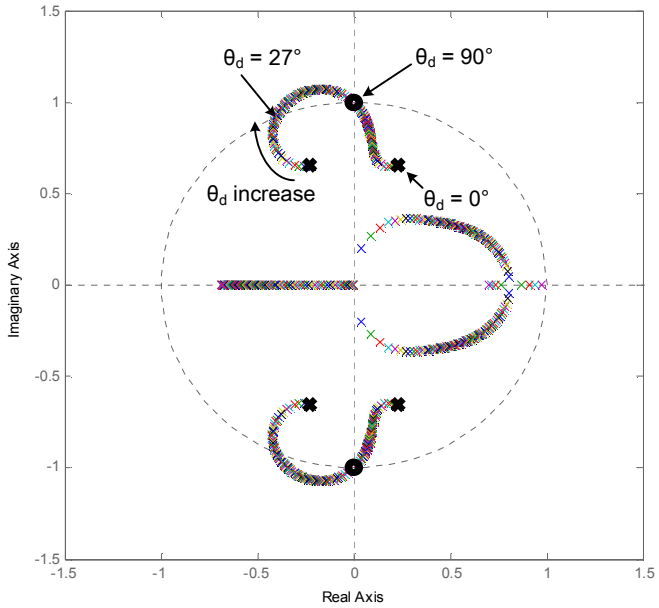


Figure 4.16 Root locus plots of the NTF for the designed 4th-order bandpass ΣΔM

of the ΣΔM. The root locus plot of the NTF in (4.24) is obtained to study the effect of the phase delay θ_d on the stability of the ΣΔM, and is shown in Figure 4.16. Clearly, as the phase delay increases, the ΣΔM tends to become instable. The root locus approaches unit circle at θ_d=27°, which can be translated to a 216-MHz 3-dB bandwidth for a single-pole gain stage. To make the phase delay negligible at 110MHz, a bandwidth of at least 1GHz is required for the amplifier, or the phase delay in the vicinity of the passband must be compensated by phase regulator as done in last chapter. In Chapter 6, a transimpedance amplifier with bandwidth enhancement is designed to achieve more than 1-GHz bandwidth at reasonable low power consumption. The resultant modified bandpass ΣΔM structure employing LCRs SAW filter is shown in Figure 4.17.

4.3.2 Other Non-Idealities in ΣΔM

Like other CT ΣΔMs, the designed LCRs SAW filter based bandpass ΣΔM is more prone to some circuit non-idealities, such as quantizer metastability, excess loop delay

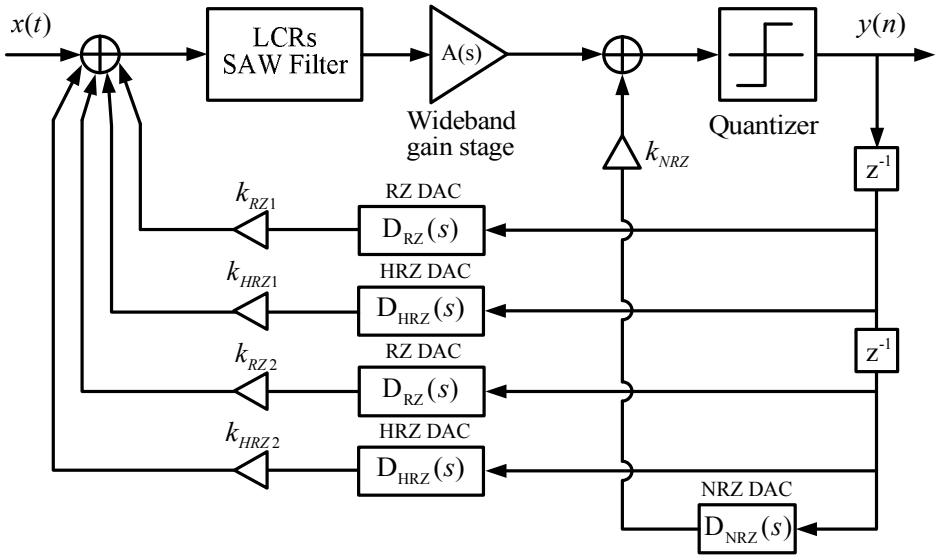


Figure 4.17 The proposed bandpass ΣΔM employing LCRs SAW filter

and clock jitter. In order to reduce the risk of the metastability, one clock period delay (realized by two cascaded master-slave ECL latches) is introduced right after the one-bit quantizer. The signal needs to go through at least 4 latches before driving any DAC, therefore the risk of having a metastable output is very low. The excess loop delay can be reduced by the similar clock scheme adopted in the electromechanical resonator based ΣΔM (section 3.4.3). By controlling the tail current of the inverting clock buffer, a programmable clock delay can be achieved to fully compensate the excess loop delay.

Clock jitter is critical to the performance of CT ΣΔMs, especially when current steering DACs (switched-current DACs) are employed. The formula in (3.19), which is repeated in (4.38)

$$SNR_{\max}(dB) = 10 \cdot \log_{10} \frac{OSR}{\alpha \cdot \frac{\sigma_{jitter}^2}{T_s^2}} \tag{4.38}$$

is used to estimate the peak SNR performance limit due to the clock jitter. It can be shown that the SNR performance in 1-MHz of the designed ΣΔM will be limited to only about 68dB, given OSR=220 and α=48 in this design, and the 2-ps rms jitter for clock

signal. To further improve the SNR performance, low-jitter clock is needed. The state-of art-clock generation circuit can achieve a jitter performance as low as 1ps at a frequency range from 200 to 500MHz. With low jitter clock (1ps), the peak SNR can be improved to about 74dB.

CHAPTER 5

IMPLEMENTATION OF ELECTROMECHANICAL RESONATORS BASED CT BANDPASS ΣΔMS

In this chapter, two generations of resonators based CT bandpass ΣΔMs are described. In the first generation, only a 2^{nd}-order modulator is realized. For the second generation, an improved 2^{nd}-order together with a 4^{th}-order ΣΔMs are demonstrated. These ΣΔM chips are fabricated in a 0.35-μm CMOS process and tested with various electromechanical resonators, including SAW (47.3-MHz, 77.25-MHz and 108-MHz) and MEMS (CC-beam, 19.6-MHz) resonators. The performance comparison with the state-of-art bandpass ΣΔMs is also given.

5.1 Circuit-level Architectures

5.1.1 The First-Generation 2^{nd}-Order Bandpass ΣΔM

The complete circuit-level implementation of the first-generation 2^{nd}-order CT bandpass ΣΔM employing electromechanical resonator is given in Figure 5.1 [130]. The electromechanical resonator and the anti-resonance cancellation capacitor are off-chip. All the other circuits are implemented on-chip in a fully differential style for common-mode noise rejection and inter-symbol interferences cancellation except for the circuits that interface with the off-chip resonator. The parasitic effects from the I/O pads and PCB have also been taken into account in both schematic and post-layout simulation using the models given by the foundry.

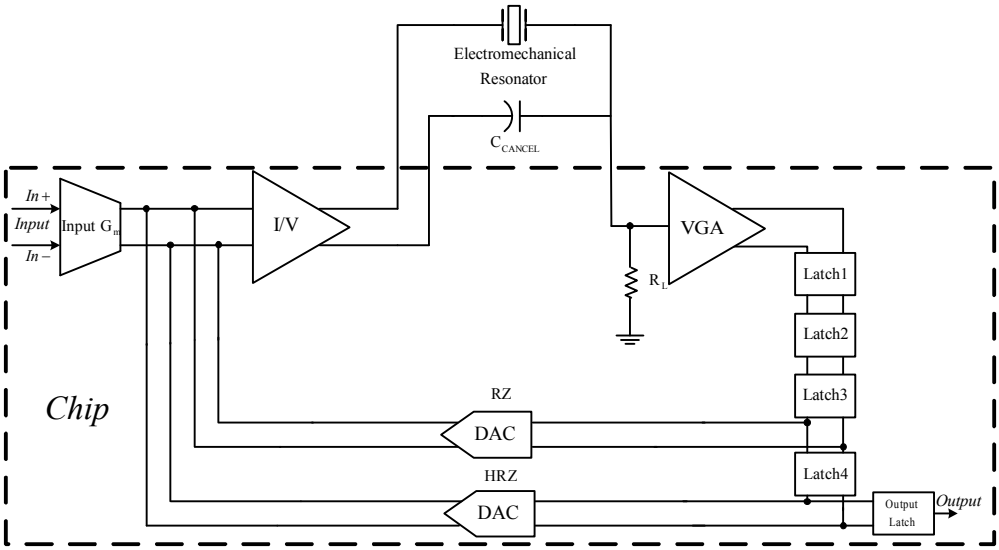


Figure 5.1 Circuit-level block diagram of the proposed first-generation 2nd-order bandpass ΣΔM

The input transconductor is used to convert the input signal from voltage to current so that the summation with the feedback signals from DACs can be performed in the current domain. After the summation, the current signal is converted back to voltage and for drive the off-chip electromechanical resonator. The output signal from the resonator is amplified and phase-compensated by a bandpass-like variable gain amplifier (VGA) before it is quantized. The quantizer and one sampling period delay, as well as the RZ and HRZ signal generators are realized with four serially connected dynamic latches. Latch1 and Latch2 act as the one bit quantizer and provide half sampling period delay. Latch3 and Latch4 generate the RZ and HRZ control signals for the current steering DACs. A slightly different circuit is used to implement Latch1 to reduce the kickback noise. The modulator's digital output is obtained from the output latch (D flip-flop) driven by Latch4.

5.1.2 The Second-Generation 2nd- and 4th-Order Bandpass ΣΔM

The circuit-level implementations of the second-generation 2nd- and 4th-order CT bandpass ΣΔMs employing electromechanical resonators [106][131][132] are given in

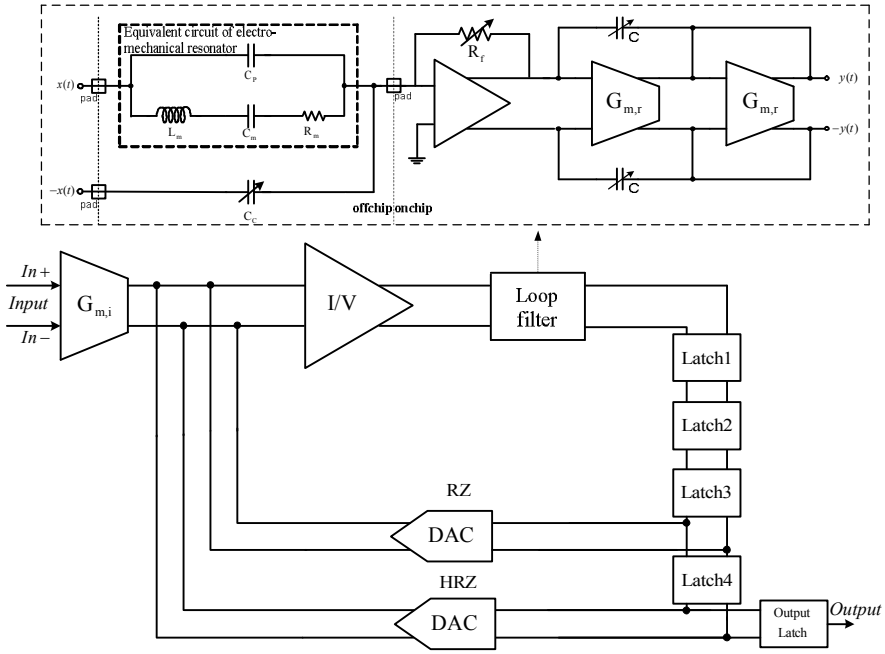


Figure 5.2 Circuit-level block diagram of the proposed second-generation 2nd-order bandpass ΣΔM

Figure 5.2 and Figure 5.3, respectively. The feedback coefficients for the 4th-order modulator are re-scaled based on the circuit parameters and sampling frequency.

$$\begin{cases} k_{RZ4} = -1.1262 \dfrac{f_s}{\dfrac{R_L}{L_m} \cdot G_{m,i} \cdot R_{I/V} \cdot A_l} \\ k_{HRZ4} = 2.7054 \dfrac{f_s}{\dfrac{R_L}{L_m} \cdot G_{m,i} \cdot R_{I/V} \cdot A_l} \\ k_{RZ2} = -1.0071 \\ k_{HRZ2} = 4.7022 \end{cases} \tag{5.1}$$

where f_s is the sampling frequency, $G_{m,i}$ is the transconductance of the transconductor before the I/V converter, $R_{I/V}$ is the equivalent input resistance of the I/V converter and A_l is the overall loop filter gain which is given below, as indicated in Figure 3.13,

$$A_l = IL \cdot A_{TIA} \cdot A_{PR} \tag{5.2}$$

where IL is the insertion loss of the electromechanical resonator, A_{TIA} and A_{PR} are the voltage gains of transimpedance amplifier and phase regulator, respectively. Most of the

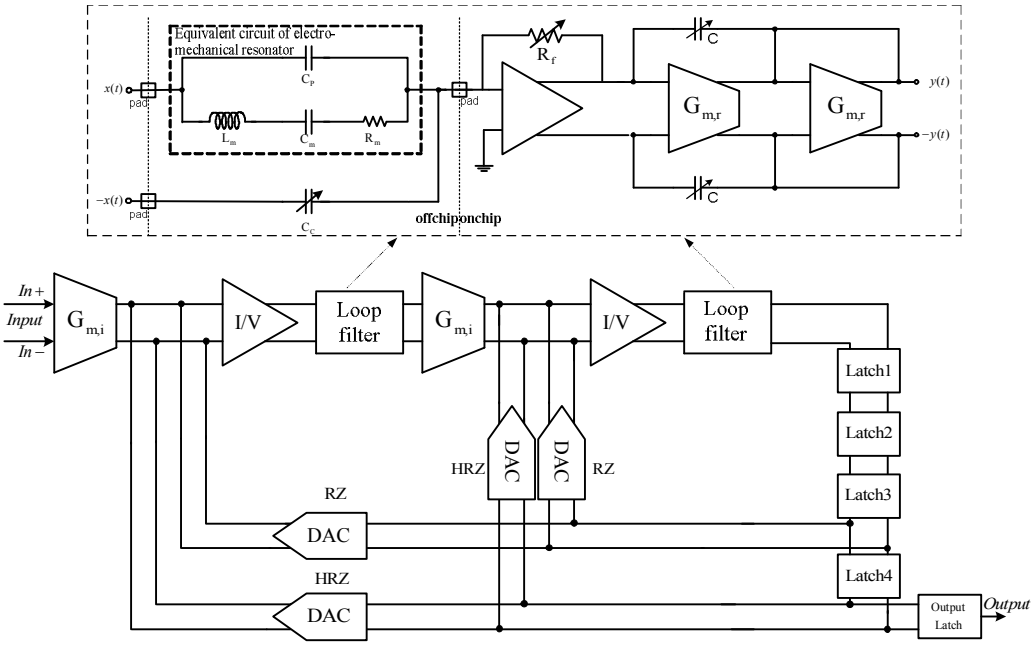


Figure 5.3 Circuit-level block diagram of the proposed second-generation 4th-order bandpass ΣΔM

circuit blocks in the second generation of 2nd-order and the 4th-order ΣΔMs, including the input transconductor, the quantizer, the output latch and the feedback DACs, are similar to those in the first-generation 2nd-order ΣΔM.

The major difference is in the sensing circuit for the off-chip electromechanical resonator and the gain stage circuit together with the phase compensation circuit, as shown in Figure 5.2 and Figure 5.3. In the first generation, the output of the electromechanical resonator is sensed by a resistor followed by a VGA in voltage domain. Since the output of the resonator is a current in nature, the sensing circuit in the second generation ΣΔMs is implemented by a wideband transimpedance amplifier (TIA) which works as the gain stage at the same time. TIA is chosen for its low input resistance and wide bandwidth. The low input impedance minimizes the degradation of loaded Q, as given in equation (3.3), and facilitates the current sensing for the resonator. The phase compensation is realized by a first-order Gm-C all-pass filter, and the amount of frequency compensation is programmable.

Table 5.1 Design specifications

Technology	0.35-μm CMOS	
Supply Voltage	3.3 V	
Type	SAW, MEMS, Crystal	
Sampling Frequency	1 GHz maximum	
Center Frequency	250 MHz maximum	
Bandwidth	200 kHz	
Modulator Order	2	4
Expected Resolution	9 bit (56dB)	12 bit (74dB)

5.2 Circuit Blocks

The bandpass ΣΔMs to be designed target a maximum sampling frequency of 1GHz. Since the center frequency of IF is always one fourth of the sampling frequency, by changing the sampling frequency, different center frequency can be realized. Moreover, the main objective of this work is to explore the feasibility of electromechanical resonators based ΣΔMs, the designs are not targeted for any application at this stage. However, to compare or benchmark this work to the others, the bandwidth of the ΣΔM is set to 200kHz. The design specifications of the bandpass ΣΔMs are listed in Table 5.1.

5.2.1 Input Transconductor

Since the input transconductor, $G_{m,i}$, is outside of the feedback loop, its performance directly impacts on the overall dynamic range of the bandpass ΣΔM [51]. Thus, the linearity of the transconductor and the input-referred in-band noise should be minimized and below the minimum resolution with certain margin. With the given dynamic range at the summing node, the transconductance value determines the full input voltage range. Meanwhile, the transconductor should also have enough bandwidth.

A inverter-based high speed transconductor first proposed in [87][133] is adopted , as shown in Figure 5.4. The transconductor has a differential architecture, made of two

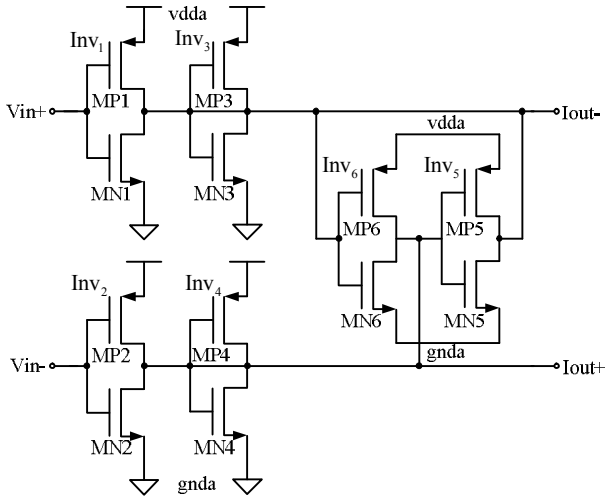


Figure 5.4 Schematic of the input transconductor

identical sub-circuits: inverters Inv_1, Inv_3, Inv_5 and inverters Inv_2, Inv_4, Inv_6, respectively. Inverters Inv_1 and Inv_2 are responsible for generating the transconductance, while inverters Inv_3 and Inv_5, Inv_4 and Inv_6 guarantee the common-mode stability (low common-mode resistance) and high differential-mode output resistance. Due to the absence of internal nodes, this transconductor can work at very high frequency up to gigahertz range in the chosen 0.35-μm CMOS technology. This transconductor delivers a linear differential transconductance $G_{m,i}$ given by

$$G_{m,i} = \mu_n C_{ox} \frac{W_{n1,2}}{L_{n1,2}} \left(V_{cm} - V_{thn}\right) + \mu_p C_{ox} \frac{W_{p1,2}}{L_{p1,2}} \left(V_{dda} - V_{cm} - V_{thp}\right) \tag{5.3}$$

as long as all of its transistors work in saturation and long channel square law of MOS transistors assumed, in which V_{cm} is the common mode voltage of input signal and $W_{n1,2}/L_{n1,2}$, $W_{p1,2}/L_{p1,2}$ are the dimension ratios for MN1/2, MP1/2, respectively. If inverter Inv_i has transconductance $g_{m\_Invi} = (g_{m\_MNi} + g_{m\_MPi})$ and small-signal output conductance $g_{o\_Invi} = (g_{o\_MNi} + g_{o\_MPi})$ [87], the common-mode output resistance is,

$$R_{cm} = \frac{1}{g_{o\_Inv1} + g_{o\_Inv3} + g_{o\_Inv5} + g_{m\_Inv3} + g_{m\_Inv5}} \tag{5.4}$$

While the differential-mode resistance at the same node is

$$R_{dm} = \frac{1}{g_{o\_Inv1} + g_{o\_Inv3} + g_{o\_Inv5} + g_{m\_Inv3} - g_{m\_Inv5}} \tag{5.5}$$

If for all i, $g_{o\_Invi} = g_{o\_Inv}$ and $g_{m\_Invi} = g_{m\_Inv}$, the common-mode and differential-mode gain at either output node is

$$A_{cm} = \frac{g_{m\_Inv}}{3g_{o\_Inv} + 2g_{m\_Inv}} < 1 \tag{5.6}$$

and

$$A_{dm} = \frac{g_{m\_Inv}}{3g_{o\_Inv}} \tag{5.7}$$

respectively. Generally, $g_m \gg g_d$ is required to obtain a reasonable high A_{dm}. Since $A_{cm} < 1$, common-mode stability can be guaranteed.

The input-referred noise density of the transconductor is calculated [87] and expressed as (flicker noise ignored)

$$V_{n\_Gm}^2 = \frac{4kT\left(\gamma\sum_{i=1}^{6} g_{m\_Invi} + \frac{1}{R_{I/V}}\right)}{G_{m,i}^2} = \frac{24kT\gamma g_{m\_Inv} + 4kT\frac{1}{R_{I/V}}}{G_{m,i}^2} \tag{5.8}$$

where $R_{I/V}$ is the input resistance of I/V converter after the current summing point (Figure 5.1-3). For small differential input, $G_{m,i} \cong g_{m\_Inv}$, thus (5.8) is reduced to

$$V_{n\_Gm}^2 = \frac{24kT\gamma}{G_{m,i}} + \frac{4kT/R_{in\_I/V}}{G_{m,i}^2} \tag{5.9}$$

Clearly, large transistor dimension is desired to minimize the input-referred noise, but results in high power consumption. A tradeoff is needed in choosing transistor size. Transistor-level simulation indicates that a $G_{m,i} > 2ms$ is good enough to keep the in-band noise power more than 90dB lower than the full scale differential input signal (400mV). A $G_{m,i} = 2.4ms$ is chosen in this design.

Many reasons may cause non-linearity in the transconductor, such the mismatch between two input inverters, short channel effect and the distortion in output conductance [87]. Therefore, long channel devices are used and careful layout is done to ensure good matching. Intermodulation simulation with two -12-dBFS tones in post-layout level indicates that IM3 better than 80dB can be achieved. The main drawback of the inverter-based transconductor is that its transconductance can only be tuned by varying the supply voltage, but this is not important in this work since the transconductance need not to be tuned.

5.2.2 VGA in the First-Generation 2nd-Order Bandpass ΣΔM

The VGA circuit provides three functions, namely, gain, phase compensation and single-to-differential conversion. As a tradeoff between stability of ΣΔM and resolution of the quantizer, the gain of the VGA should be around 15~40dB, as indicated in section 3.3.2. The schematic of the VGA, which is similar to the one in [134], is given in Figure 5.5. It is essentially a Gilbert cell with lowpass feedback network to suppress the DC offset. The gain is controlled by Vc. MN2, MN5-6, and MN11-12 form a negative

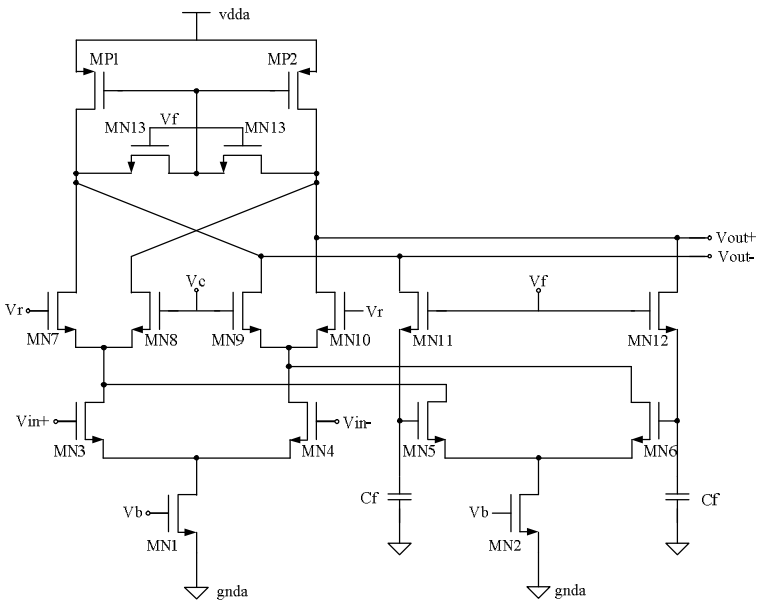


Figure 5.5 Schematic of the VGA

feedback with a lowpass filter to cancel the DC offset and provide a leading phase for the purpose of phase delay compensation. The lowpass filter is formed by MN11, MN12 which work in triode region, and C1, C2. The Gilbert gain stage without the negative feedback network can be simply modeled by a single-pole lowpass transfer function $A(s)$, that is

$$A(s) = \frac{g_{ma} R_L}{1 + \dfrac{s}{\omega_{-3dB,main}}} \tag{5.10}$$

The feedback path can also be modeled by a lowpass function $B(s)$ with unit DC gain, given by

$$B(s) = \frac{1}{1 + \dfrac{s}{\omega_{-3dB,f}}} \tag{5.11}$$

where g_{ma} is the transconductance of MN3 and MN4, R_L is loading resistance at output node, $\omega_{-3dB,main}$ and $\omega_{-3dB,f}$ are 3-dB bandwidth frequencies of the main amplifier and the feedback network, respectively. The close-loop transfer function of the VGA is derived to be

$$H(s) = \frac{g_{ma} R_L}{1 + g_{mb} R_L} \cdot \frac{1 + \dfrac{s}{\omega_{-3dB,f}}}{1 + \dfrac{s}{\omega_0 Q} + \dfrac{s^2}{\omega_0^2}} \tag{5.12}$$

$$\omega_0 = \sqrt{(1 + g_{mb} R_L) \cdot \omega_{-3dB,main} \omega_{-3dB,f}} \approx \sqrt{\omega_T \omega_{-3dB,f}} \tag{5.13}$$

$$Q = \frac{\omega_0}{\omega_{-3dB,main} + \omega_{-3dB,f}} \tag{5.14}$$

where ω_T is the unit gain bandwidth of the main amplifier, and g_{mb} is transconductance of MN5 and MN6. It is clear from equation (5.12) that the close-loop VGA is a bandpass system with a center frequency at ω_0. Considering the DC offset cancellation, the

output-referred offset voltage can be cancelled by minimizing the DC gain, which is given from equation (5.12) as

$$H_0 = \frac{g_{ma}R_L}{1+g_{mb}R_L} \tag{5.15}$$

To trade off among power, area, noise and output offset, g_{mb} is set to the same as g_{ma}. Therefore, the close-loop DC gain is approximately 0 dB, and the offset voltage will not be amplified. Furthermore, the phase of the VGA can be expressed as

$$\varphi = \tan^{-1}\frac{\omega_0}{\omega_{-3dB,f}} - \tan^{-1}\frac{\omega_0}{\omega_{-3dB,main}} - \tan^{-1}\frac{\omega_0}{(1+g_{mb}R_L)\omega_{-3dB,f}} \tag{5.16}$$

Since $(1+g_{mb}R_L)\omega_{3dB,f}$ is much greater than $\omega_{3dB,main}$, the contribution from the last term in (5.16) can be ignored and the overall phase can be made leading by adjusting $\omega_{-3dB,f}$, which is determined by

$$\omega_{-3dB,f} \approx \frac{1}{R_{on}(C_f + C_{gs5,6})} \tag{5.17}$$

where R_{on} is the on-resistance of MN11 and MN12 in the triode region. The amount of the phase compensation can be controlled by V_f, which changes the value of R_{on}. The goal of the phase compensation is to make the overall phase delay of the VGA close to zero. The typical magnitude and phase response of the VGA from post-layout simulation

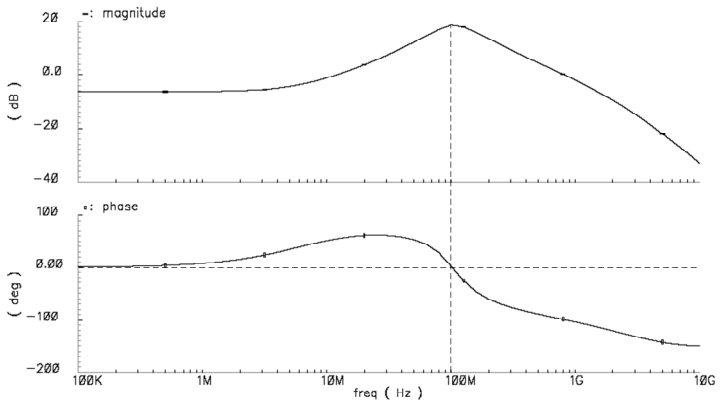


Figure 5.6 Simulated frequency response of the VGA

is given in Figure 5.6, where $\omega_0 = 100\text{MHz}$.

5.2.3 TIA and Phase Regulator in the Second-Generation Bandpass ΣΔMs

In the second-generation designs, VGA is replaced by a TIA. The schematic of the TIA is depicted in Figure 5.7. The bandwidth of the TIA is mainly determined by the dominant pole at its input, which is greatly affected by the parasitic capacitances (C_p) at the output port of the resonator, together with the capacitances from the chip package and bonding pad (~2pF). Therefore, the main gain (transimpedance) stage (MN3) is preceded by a source follower (MN1 and MN2) which prevents the Miller capacitance of the gain stage from adding onto the input terminal and enhances the overall bandwidth. The feedback resistor is implemented via a voltage-controlled PMOS transistor, MP1, operating in the triode region and thus allows the gain of the transimpedance amplifier to be adjusted. A lowpass filter is used to generate a pseudo differential signal for the following differential pair and hence a differential output is obtained. The lowpass filter is formed by a long channel PMOS transistor MP3 and capacitor C.

The open-loop DC gain of the TIA is approximated by

$$A_{DC} \approx g_{m3} R_L \tag{5.18}$$

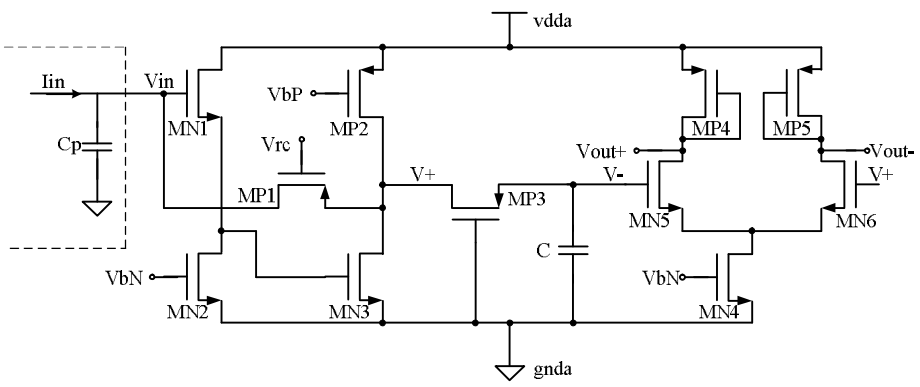


Figure 5.7 Schematic of the TIA

where g_{m3} is the transconductance of MN3, respectively and R_L is the load at output node of the gain stage. Therefore the input resistance can be approximated as

$$R_{in} = \frac{R_f + R_L}{1 + A_{DC}} \tag{5.19}$$

where R_f is on-resistance of MP1 in triode region. The 3-dB bandwidth is

$$\omega_{-3dB,close} = \omega_{-3dB,open} \cdot (1 + A_{DC}) \tag{5.20}$$

In which $\omega_{-3dB,open}$ is the open-loop 3-dB bandwidth, which in this work is determined by the dominated pole at the input. If the A_{DC} is properly chosen, we can obtain the reasonable low input resistance and large bandwidth. With all the parasitic effects taken into account, the post-layout simulation shows that the TIA has a typical input resistance of 120Ω, Therefore, the loaded Q of the SAW resonator is about 170 (including the parasitic resistance from the bondpad and PCB). The transresistance and the bandwidth of the TIA are 70dBΩ and 524MHz, respectively.

The effects of the parasitic greatly reduce the bandwidth of the TIA. As discussed in section 3.3.3, phase delay compensation circuit must be used to guarantee the stability of the ΣΔM. In the second-generation 2nd-order and 4th-order bandpass ΣΔMs, the compensation is accomplished by an individual phase regulator, which is a Gm-C allpass filter, as shown in Figure 5.8. If two transconductors are assumed to have same transconductance, $G_{m,r}$, the transfer function of the allpass filter is given by

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{s - 2G_{m,r}/C}{s + 2G_{m,r}/C} \tag{5.21}$$

The transition frequency can be adjusted by changing the capacitance value (coarse) and transconductance (fine), so does the phase compensation. In this work, each capacitor in the phase regulator is realized by a capacitor bank that can be tuned by a 4-bit control

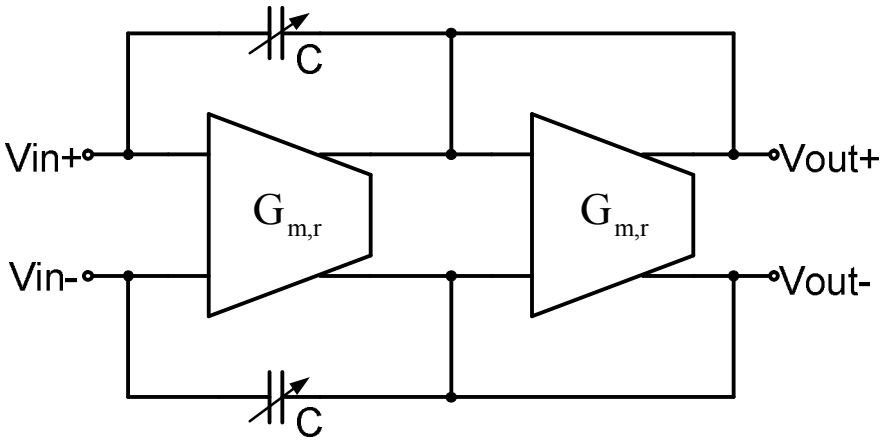


Figure 5.8 Schematic of the phase regulator (Gm-C allpass filter)

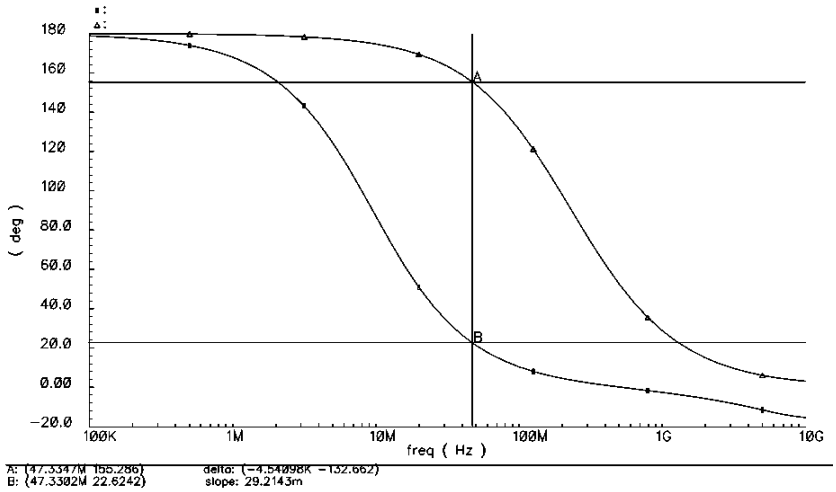


Figure 5.9 Simulated phase response of the phase regulator

word (16 different levels). The amount of the phase compensation is more than 130 degrees, as shown in Figure 5.9.

The transconductors in this allpass filter is similar to the input transconductor in section 5.2.1, the only difference is that the transconductance of the transconductors here can be varied by adjusting the supply voltage.

5.2.4 Regenerative Latches

The design of regenerative latches in Figure 5.1 to 5.3 is critical and has significant impact on the overall performance of the bandpass ΣΔMs. They must be sensitive

enough to resolve small input signals. This requires low input offset and hysteresis. They should also be able to operate at a high speed (up to 1-GHz clock in this work). Figure 5.10(a) shows the schematic of the latch used for Latch 2-4 in Figure 5.1 to 5.3.

During the track phase, i.e. when CLK goes low, transistor MN1 is cut off and the transistor pair of MN2 and MN3 is disabled. The outputs Out- and Out+ will be pulled to vdd by transistors MP1 and MP4, respectively. During the latch phase, i.e. when CLK goes high, transistor MN1 is turned on and MN2 and MN3 are enabled. At the same time, MP1 and MP4 are cut off. A small input signal causes the drain current imbalance in MN1 and MN2, which starts the regenerative process. Eventually, the input signal is latched and a valid output is produced. Although this latch can work very fast, it has high kickback noise and reduces the resolution of the quantizer. The high kickback noise of this latch is due to the fact that both clock signal and outputs can be coupled to inputs via parasitic capacitances. To reduce the kickback noise, a slightly different circuit is used to implement Latch 1, as shown in Figure 5.10(b). In this latch, the input transistors are at the bottom, only the noises from outputs are coupled to inputs. The simulated transient

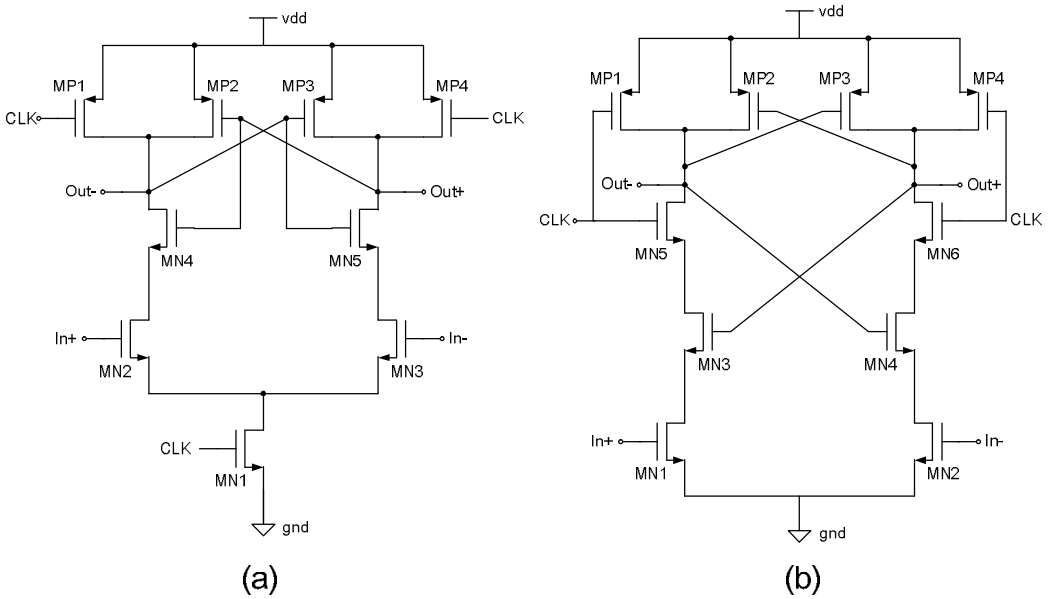


Figure 5.10 Schematics of (a) Latch2-4 and (b) Latch1

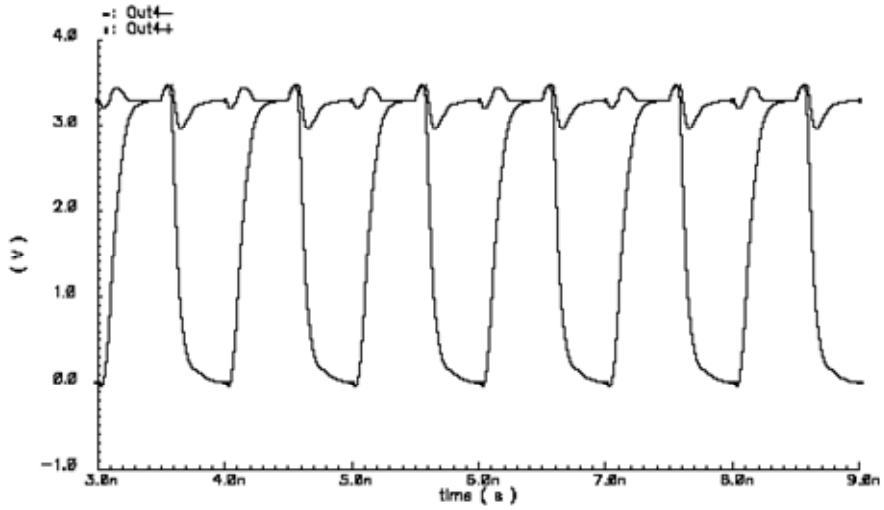


Figure 5.11 Transient response of the 4 cascaded latches

response of the four cascaded regenerative latches is shown in Figure 5.11 for inputs of $\text{In+} = 1.651V$ and $\text{In-} = 1.650V$ when clocked at 1GHz. Further Monte Carlo simulation indicates that the simulated input offset and hysteresis are ±3mV and 5mV, respectively, at input of Latch 1. These quantizer related non-idealities have negligible impact on the performance of the modulator given a typical 30-dB loop filter gain for 2^{nd}-order modulator and 50-dB loop filter gain for 4^{th}-order modulator, as discussed in chapter 3.

5.2.5 Current Steering DACs

The feedback DACs are implemented by fully differential current steering DAC, as shown in Figure 5.12. To reduce the glitches at the output, swing reduction drivers (SRDs) are used to buffer the outputs of latches 3-4 and drive the DAC switches. The swings of the driving signals are adjusted so that they are just enough to steer the current from one side to the other. The reduction of the swing also improves the operation speed of the DACs by reducing the transition time of the switches. The operation of SRD circuit is quite simple. The input inverter (MS1 and MS2) determines whether MS3 is on or off, which is in parallel with MS5. MS4 and MS5 serve as a voltage divider at output. The simulated transient response of the four cascaded regenerative latches together with

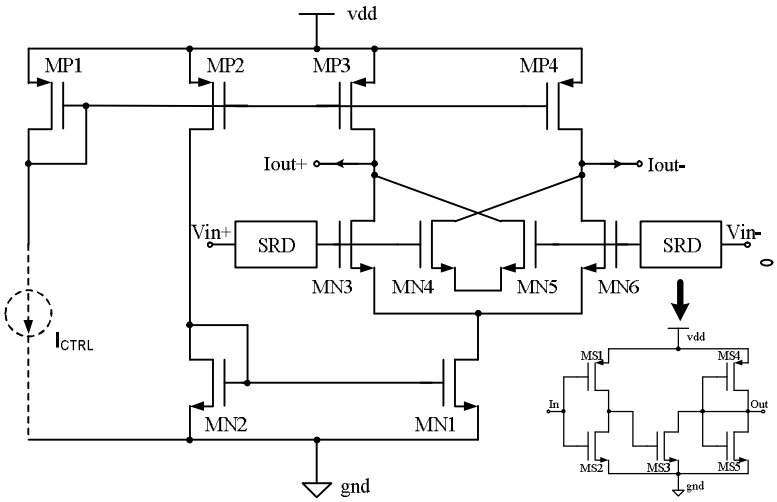


Figure 5.12 Schematic of the current steering 1-bit DAC

the SRD circuits is shown in Figure 5.13. The signal swing is reduced to 0.67V from 3.3V. The output signals of SRDs drive the NMOS differential pair, MN3 and MN6, which steer the tail current to one side or the other according to the output of the quantizer. During the track phase, Vin+ = Vin- =1.8V, as shown in Figure 5.13, the tail current is shared equally between both paths. MN4 and MN5 are two dummy transistors and used to cancel the feedthrough charges from two switches MN3 and MN6 [135]. Since the sources of MN4 and MN5 are floating, they don't contribute any current to the output of the DAC. To ensure cancellation, MN4 and MN5 have the same dimension as MN3 and MN6.

As mentioned before, current steering DAC is another source of noise that directly appears at the input of the ΣΔM. The noise of the DAC varies depending on its state. During the track phase Latch 3 or Latch 4, MN3 and MN6 conduct same current, the input-referred noise of the ΣΔM due to the DAC is

$$V_{n\_DAC\_track}^2 = \frac{4kT\gamma\left(2g_{m\_MP3/4} + 2g_{m\_MN3/6}\right)}{G_{m,i}^2} \tag{5.22}$$

where $G_{m,i}$ is the transconductance of the input transconductor. When the switch is switched to one side, the DAC noise is

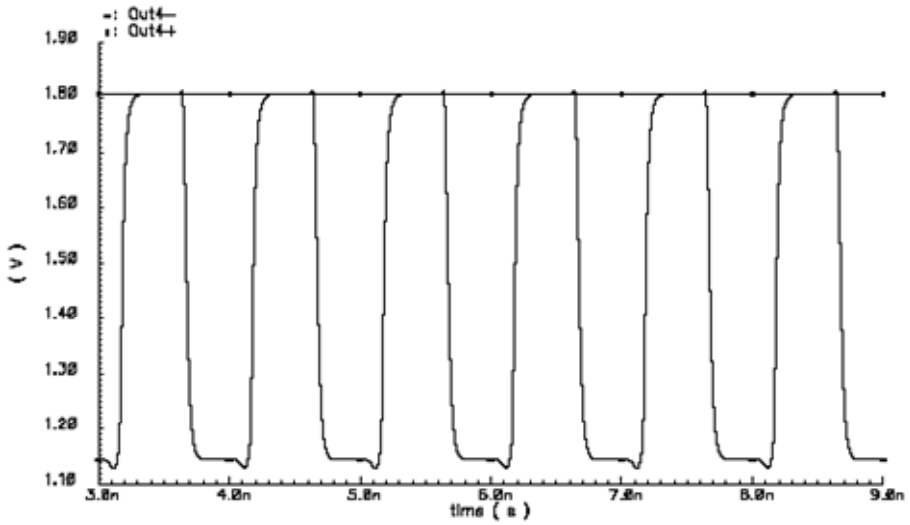


Figure 5.13 Simulated transient response at the outputs of SRDs

$$V_{n\_DAC\_switch}^2 = \frac{4kT\gamma\left(g_{m\_MP3/4} + g_{m\_MN1} + \dfrac{g_{m\_MN3/6}}{\left(1+g_{m\_MN3/6}r_{o\_MN1}\right)^2}\right)}{G_{m,i}^2} \tag{5.23}$$

Therefore, the average DAC noise is given by

$$V_{n\_DAC}^2 = \frac{1}{2}\left(V_{n\_DAC\_track}^2 + V_{n\_DAC\_switch}^2\right) \tag{5.24}$$

Large transistor aspect ratio and DAC current are preferred for low input-referred noise, but they must be traded off with power consumption and switching speed.

A noise simulation in post-layout level for the entire 4th-order bandpass ΣΔM indicates that SNR considering only device noise is 82dB in 200-kHz bandwidth, which is 8dB lower than the specification given in Table 5.1.

5.2.6 Output Latch

In order to convert the RZ output of the Latch 4 to a NRZ output which is preferred in measurement, a D flip-flip is added after Latch 4. Due to the high speed requirement (up to 1-GHz clock), a true-single-phase-clocked (TSPC) dynamic D flip-flop [136] is

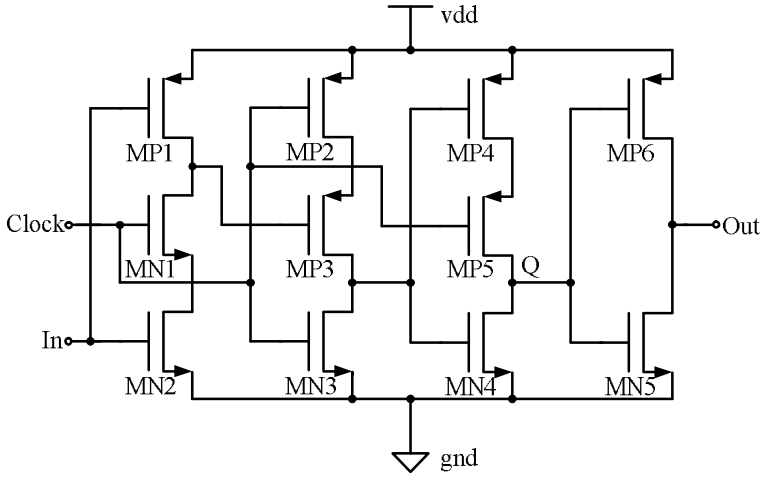


Figure 5.14 Schematic of the output latch

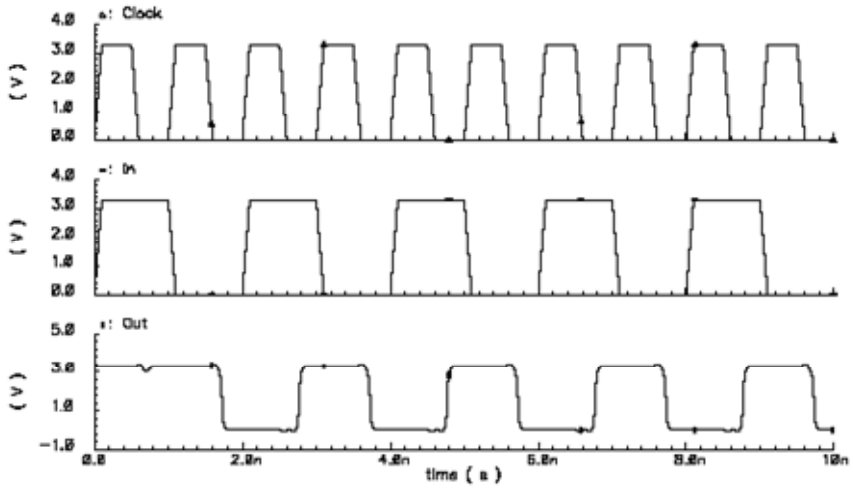


Figure 5.15 Simulation result of the output latch

chosen. Figure 5.14 shows the schematic of the TSPC D flip-flop followed by an inverter as an output buffer (formed by MN5 and MP6).

When Clock signal is high, the transistors MP2 and MP5 are cut off and the transistors MN1 and MN3 are turned on. The drain voltage of MN3 is pulled down to ground and hence forces MN4 to cutoff. The node Q becomes high impedance, thus the output is latched to the previous value. On the other hand, the transistors MN1, MN2 and MP1 form a clock buffer inverter. When the Clock signal is high, the inverter is enabled

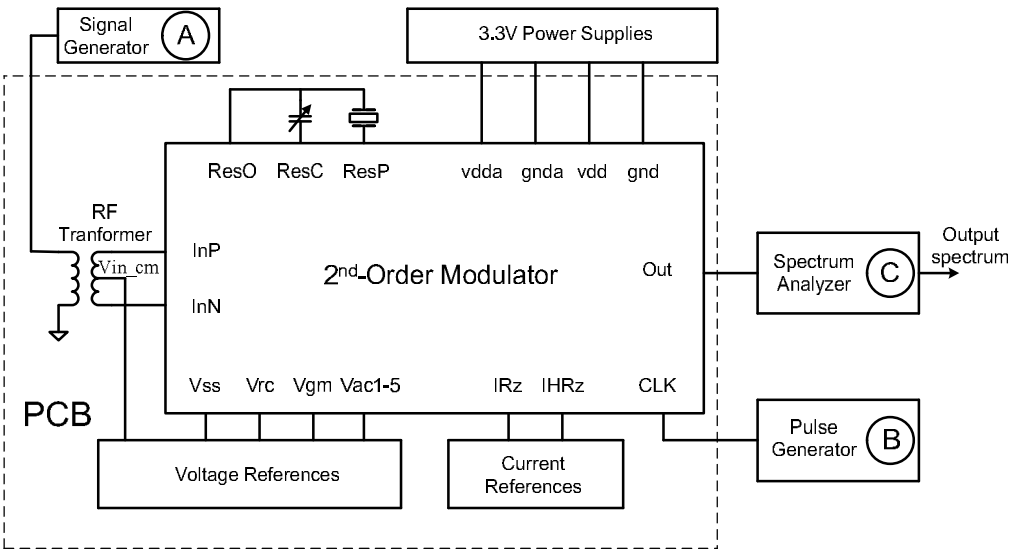
and the data passes the inverter and is stored on the gate of MP3, but with the opposite sign. When Clock signal is low, the transistors MN1 and MN3 are cut off and the transistors MP2 and MP5 are turned on. The inverter formed by MN1, MN2 and MP1 is disconnected since MN1 is off, the data stored on the gate of MP3 passes to the output. Figure 5.15 shows the simulation result at 1-GHz clock.

5.3 Measurements

The prototype ΣΔMs employing electromechanical resonators, both the first- and second-generation, are fabricated in a standard 0.35-μm, double-poly, and quadruple-metal CMOS process. This section presents the test setup and the measured results.

5.3.1 Test Setup

As an example, the experimental test setup for the second generation 2nd-order bandpass ΣΔM is shown in Figure 5.16. Similar setups are used to test for the other two



A: Agilent EE4437B Signal Generator, 250KHz-4GHz
B: Agilent 8133A Pulse Generator, 3GHz
C: Agilent E4407B Spectrum Analyzer, 9KHz-26.5GHz

Figure 5.16 Experimental test setup of the second-generation 2nd-order modulator

ΣΔMs. Several issues are considered in designing the PCB. These include power supply decoupling, voltage/reference generation, single-ended to differential conversion for input signal, and test flexibility. The testing PCBs are two-side, copper-clad boards with separate analog and digital power supplies (Appendix A). The prototype chip is soldered directly onto the PCB to minimize the parasitics from the PCB.

The differential input to the DUT is generated by driving an external, center-tapped RF transformer from a low phase noise, single ended sinusoidal signal generator. The differential sinusoidal output of transformer is applied directly to the inputs of the DUT pins, InP and InN. The common-mode voltage, V_{in_cm}, of the differential input is set to 1.65V. Four reference voltage generation circuits, as shown in Figure 5.17(a), are used to provide the DC voltage for V_{in_cm}, Vss (analog ground), Vrc, and Vgm of the modulator. Two reference current generation circuits are used to generate the bias currents for feedback DACs, as shown in Figure 5.17(b).

The electromechanical resonator and the anti-resonance cancellation capacitor are placed as close to the DUT as possible to reduce the interference from other sources. The

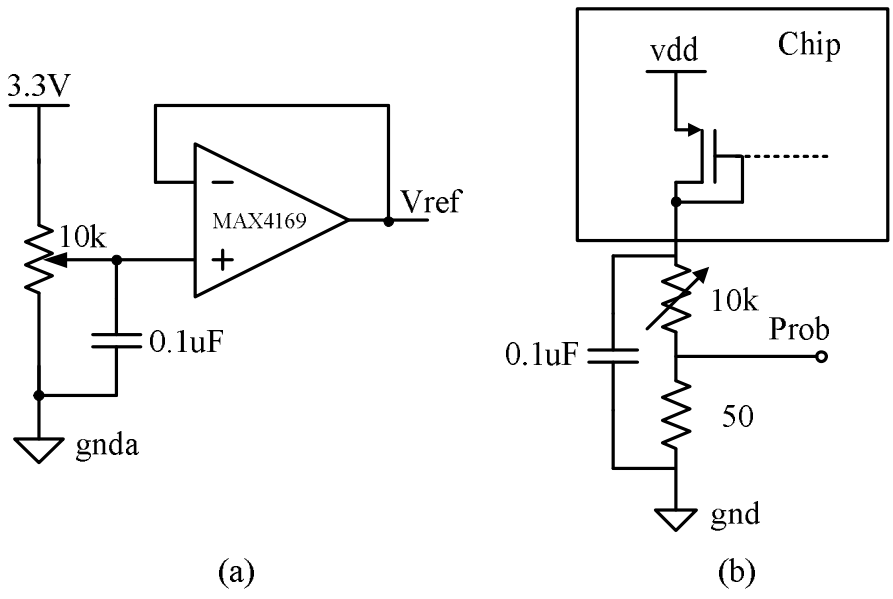


Figure 5.17 (a) Voltage and (b) current reference generation circuits

clock signal is generated by a low-jitter pulse generator. A spectrum analyzer is used to observe the output of the ΣΔM. To drive the 50-Ω resistance at the input port of the spectrum analyzer, an on-chip open-drain output buffer with high current driving capability and low output swing is used. To improve the quality of the test, it is desirable to use an oscilloscope with high sampling speed and large memory depth to capture the output bit stream of the ΣΔM. The acquired data can be post-processed, such as in Matlab, to obtain the performance of the ΣΔM under test. Unfortunately, such a high speed oscilloscope is not available at the time of the chip evaluation.

5.3.2 Experimental Results of the 1st-Generation 2nd-Order Bandpass ΣΔM

The die microphotograph of the chip is shown in Figure 5.18. The chip is driven by single clock whose frequency is set to 4 times of the center frequency (resonant frequency of the resonator). The electromechanical resonator and the capacitor for anti-

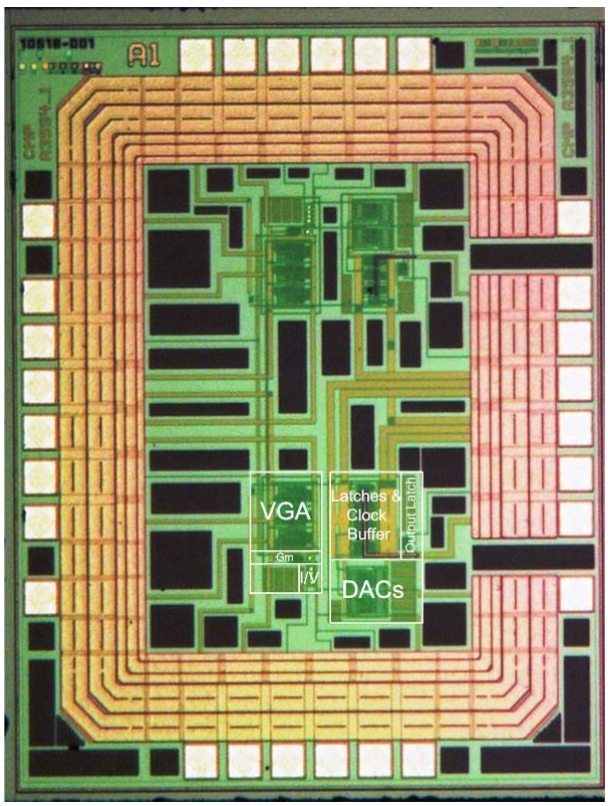


Figure 5.18 Microphotograph of first-generation ΣΔM chip

resonance cancellation are off chip. Due to the limited available off-shelf resonators, the chip was only tested with a 47.3-MHz SAW resonator and a 30-MHz crystal resonator, respectively.

Figure 5.19 shows the output spectrum of 47.3-MHz SAW resonator based bandpass ΣΔM. The corresponding SNDR plot is given in Figure 5.20. The measured dynamic range and peak SNDR in a 200-kHz signal band are 51dB and 48dB, respectively, when sampled at 189.2MHz, corresponding to a near 8-bit resolution. A similar test was also carried out for the 30-MHz crystal resonator. The measured dynamic range and peak SNR are 48dB and 44dB, respectively, slightly lower than those of SAW resonator based ΣΔM. These performance degradation could be attributed to the low oversampling ratio (OSR = 300 as opposed 473 in the case of SAW resonator).

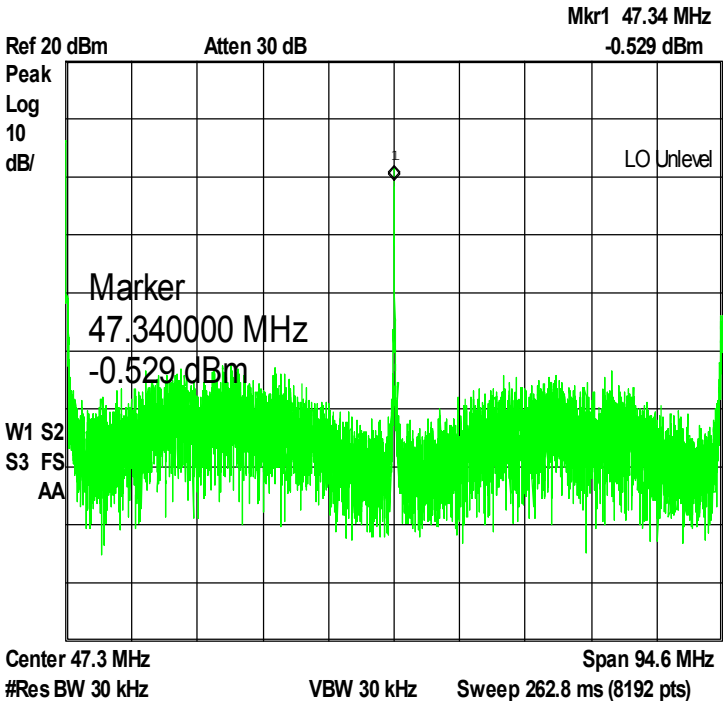


Figure 5.19 Measured output spectrum of the first-generation 2nd-order bandpass ΣΔM with a 47.3-MHz SAW resonator

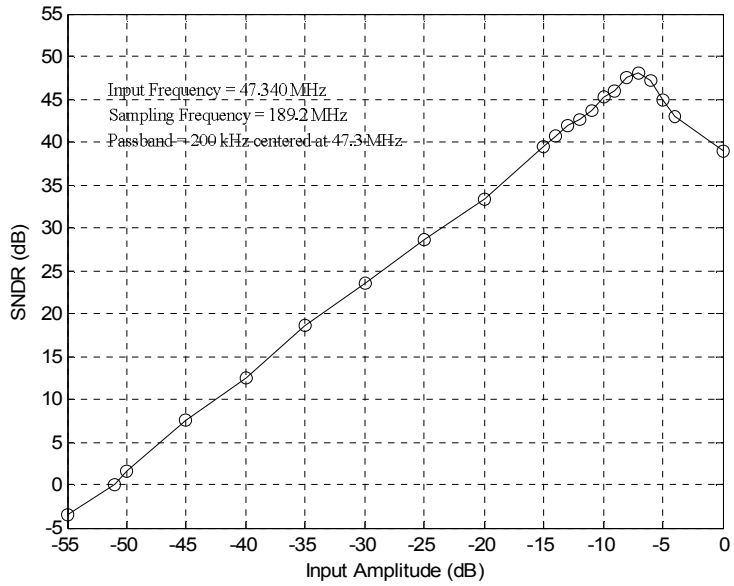


Figure 5.20 Measured SNDR plot of the first-generation 2nd-order bandpass ΣΔM

Table 5.2 Performance summary of the first-generation 2nd-order SAW/crystal resonator based bandpass ΣΔM

Technology	0.35-μm CMOS	
Supply Voltage	3.3 V	
Power	60 mW	56 mW
Modulator Order	2	
Type	SAW	Crystal
Sampling	189.2 MHz	120 MHz
Center Frequency	47.3 MHz	30 MHz
Bandwidth	200 kHz	
OSR	473	300
Dynamic Range	51 dB	48 dB
Peak SNDR	48 dB	44 dB

Table 5.2 summarizes the measured performance.

This 2nd-order ΣΔM is only the first attempt to implement CT bandpass ΣΔM employing electromechanical resonator. Even though the performance is not quite satisfying, a functional bandpass ΣΔM based on SAW or crystal resonator is successfully demonstrated and it proves the proposed concept.

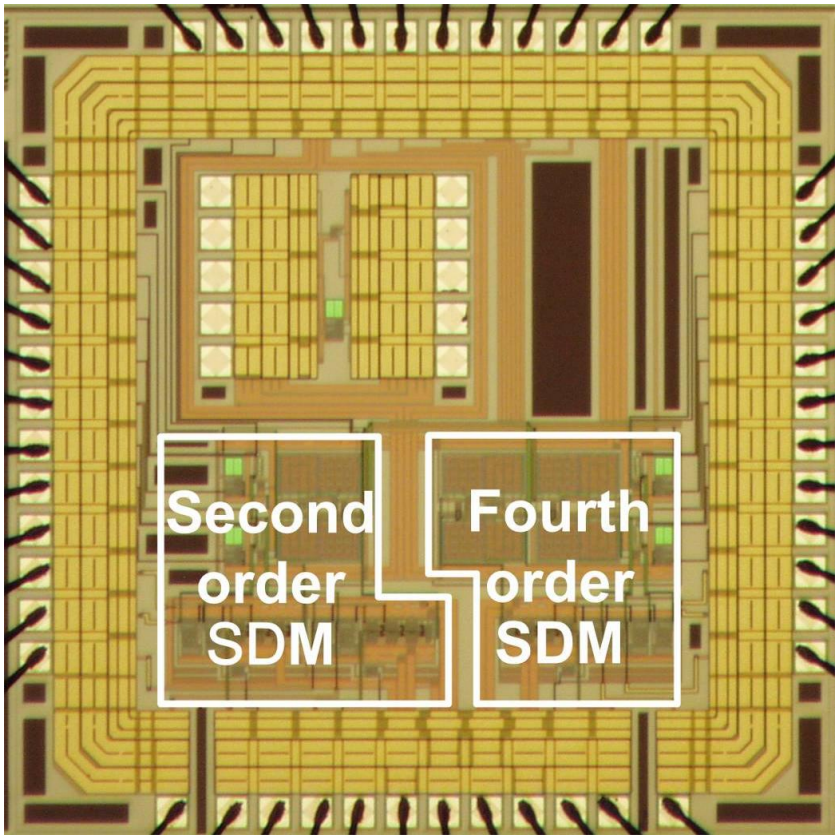


Figure 5.21 Microphotograph of second-generation ΣΔM chip

5.3.3 Experimental Results of the 2nd-Generation 2nd-Order Bandpass ΣΔM

The microphotograph of the second-generation ΣΔMs chip is shown in Figure 5.21, which consists of a 2nd- and a 4th-order modulator. The fabricated chip is mounted in a TQFP-48 package and soldered directly onto the PCB to avoid the unnecessary parasitic. The electromechanical resonator and the cancellation capacitor are off-chip and placed as close to the modulator chip as possible, to reduce the wiring parasitics. The 2nd-order ΣΔM is tested with 47.3-MHz, 77.25-MHz, 108.7-MHz SAW resonators and a 19.6-MHz CC-beam silicon MEMS resonator, respectively.

Figure 5.22 shows the measured output spectrum of the second-generation 2nd-order bandpass ΣΔM with a 47.3-MHz SAW resonator. The measured peak SNDR and dynamic range in a 200-kHz bandwidth centered at 47.3MHz are 54dB and 57dB, respectively, as depicted in Figure 5.23.

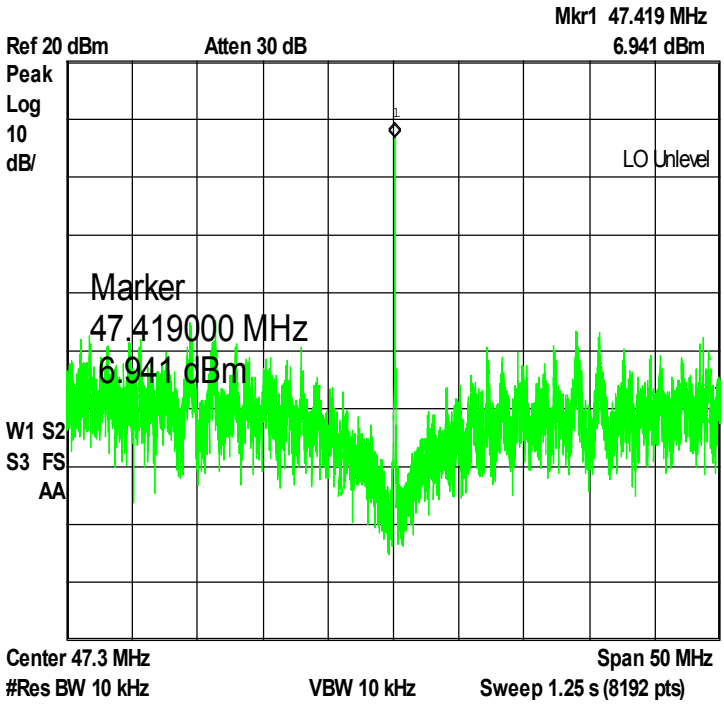


Figure 5.22 Measured output spectrum of the second-generation 2nd-order bandpass ΣΔM with a 47.3-MHz SAW resonator

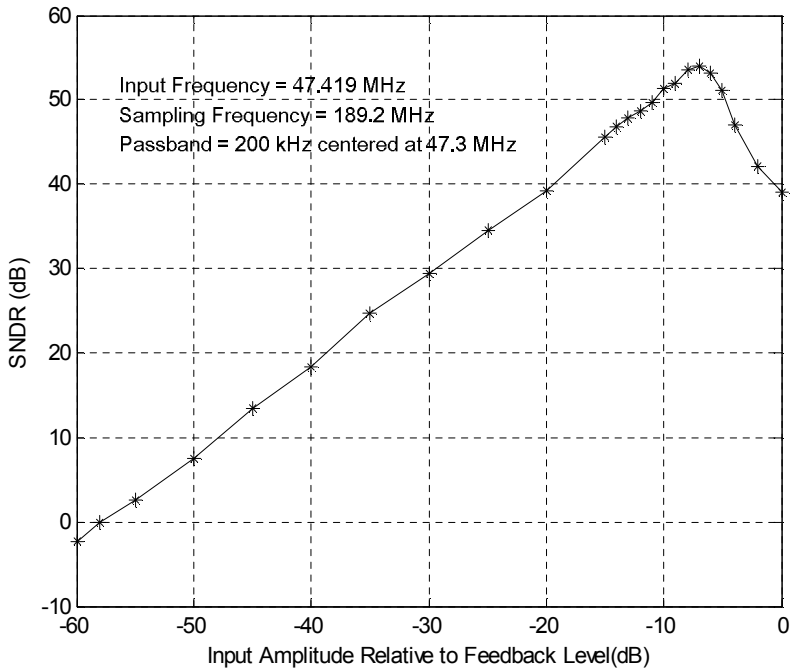


Figure 5.23 Measured SNDR plot of the second-generation 2nd-order bandpass ΣΔM

Compared with the first generation, the second generation improves the performance by 6dB or 1bit. The improvement is attributed to the better resonator sensing circuit and the more precise controllability of the phase delay compensation circuit, which is evident by the much deep noise-shaping shown in Figure 5.24. This is because the phase shift compensation circuit in the second-generation ΣΔM has wide tunability to completely compensate the excess phase delay in the forward path. The comparison with the previously reported 2nd-order single-bit CT and DT bandpass ΣΔMs is given in Table 5.3. A figure of merit (FOM) similar to that proposed in [85] is also used for comparison. The FOM is defined as

$$FOM = SNDR_{dB} + 10\log\left(\frac{BW}{P}\right) \tag{5.25}$$

where BW is the signal bandwidth and P is the power consumption. The proposed second generation 2nd-order ΣΔM in this work achieves better FOM and SNDR, even when compared with DT ΣΔMs. The above measured results have demonstrated the

Table 5.3 Performance comparison of the second-generation 2nd-order SAW resonator based bandpass ΣΔM with previously published work

Design	**This Work**	[24]	[28]	[25]	[61]	[63]	[7]
Process	**0.35-μm CMOS**	0.8-μm BiCMOS	0.5-μm CMOS	0.5-μm Bipolar	0.35-μm CMOS	1.2-μm BiCMOS	0.8-μm BiCMOS
Supply Voltage	**3.3V**	5V	3V	5V	1V	5V	5V
Type	**SAW**	Gm-C	Gm-C	LC	SC	SC	SC
Power	**30mW**	>100mW	47mW	135 mW	12mW	30mW	60mW
Sampling Frequency	**189.2MHz**	200MHz	280MHz	3.8GHz	42.8MHz	42.8MHz	42.8MHz
Center Frequency	**47.3MHz**	50MHz	70MHz	950MHz	10.7MHz	10.7MHz	10.7MHz
Bandwidth	**200kHz**	200kHz	200kHz	200kHz	200kHz	200kHz	200kHz
OSR	**473**	500	700	9500	107	107	107
Dynamic Range	**57dB**	N/A	N/A	N/A	N/A	N/A	57dB
Peak SNDR	**54dB**	46dB	42dB	49dB	42.3dB	46dB*	47dB*
FOM	**122.24**	<109	108.29	110.71	114.52	114.24	112.23

"*": denote only peak SNR performance reported

feasibility of realizing electromechanical resonator based CT bandpass ΣΔM and shown that it has the potential to achieve superior performance.

The measurements with other SAW resonators having higher resonant frequencies

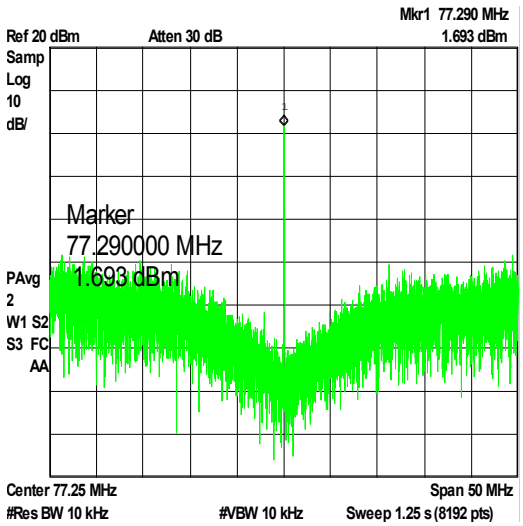


Figure 5.24 Measured output spectrum of the second-generation 2nd-order bandpass ΣΔM with a 77.25-MHz SAW resonator

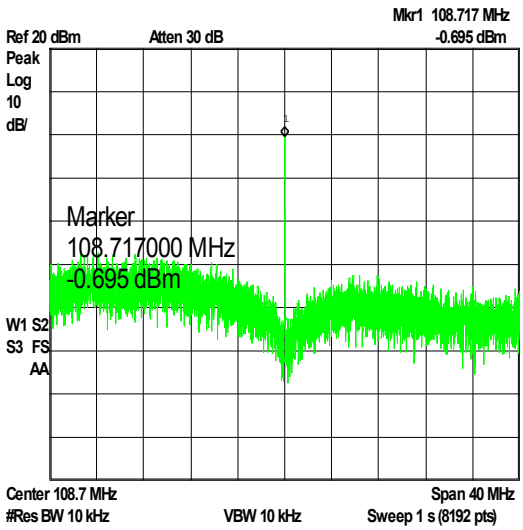
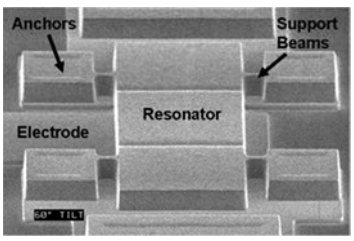


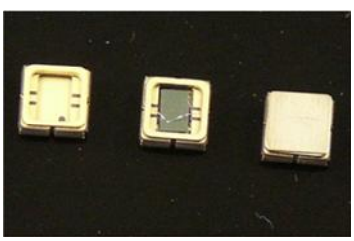
Figure 5.25 Measured output spectrum of the second-generation 2nd-order bandpass ΣΔM with a 108.7-MHz SAW resonator

(77.25MHz and 108.7MHz) are also conducted to evaluate its high speed performance. The measured output spectra are shown in Figure 5.24 for the 77.25-MHz resonator and Figure 5.25 for the 108.7-MHz resonator, respectively. The measured output spectrum with the 77.25-MHz SAW resonator indicates that this modulator can achieve comparable SNDR performances compared with that with 47.3-MHz SAW resonator. However, for the 108.7-MHz resonator, its SNDR is only around 40dB in a 200-kHz signal bandwidth. This degradation is likely the results of worse excess loop delays both in forward and feedback paths at higher frequencies. Attempt has been made to compensate the loop delays by adjusting the phase compensation in forward path and DAC coefficients in feedback path. Unfortunately, it doesn't work well, since the loop delays at 108.7MHz may already exceed the tuning range. In addition, the poor speed performance of the output buffer pad provided by the foundry may be partially responsible for the performance degradation at higher center frequencies.

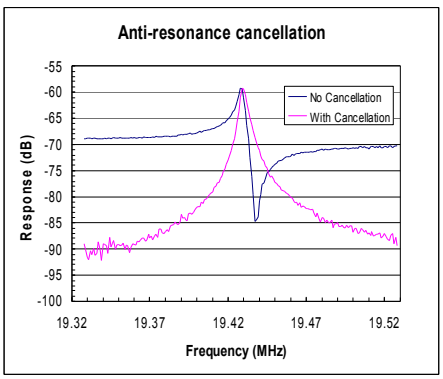
The silicon MEMS resonator used in the testing is a clamp-clamp type resonator and comprises a resonator beam made of 2-μm thick polysilicon and supported by four support beams, as shown in Figure 5.26. One end of each support beam is connected to



Micrograph of M-resonator



Resonator chip in package



Frequency response measured with 50Ω load

Figure 5.26 Silicon MEMS resonator and measured magnitude response

the resonator beam while the other end is anchored to the substrate. For operation, a DC bias voltage of 2~5V is applied on the resonator beam while an AC input signal is applied on the electrode that is placed underneath the resonator beam with about 100-nm air gap. The resonator chip is placed in a 3mm × 3mm ceramic package and sealed in vacuum environment (10mTorr). The typical measured magnitude response with a 50-Ω load is shown in Figure 5.26. The quality factor under certain vacuum condition is larger than 2000. The notch above the resonant frequency in the magnitude response is referred to as anti-resonance at which the resonator is in parallel resonant mode.

The measured output spectrums from the ΣΔM are shown in Figure 5.27. The SNDR plot is shown in Figure 5.28. The 0-dB input level corresponds to 400mV. The measured peak SNDR is 51dB and dynamic range is 52.5dB for a 200-kHz signal bandwidth. The ΣΔM has a power consumption of 28mW under 3.3-V supply. Note that this design is not optimized for the low power consumption. Further reduction of the

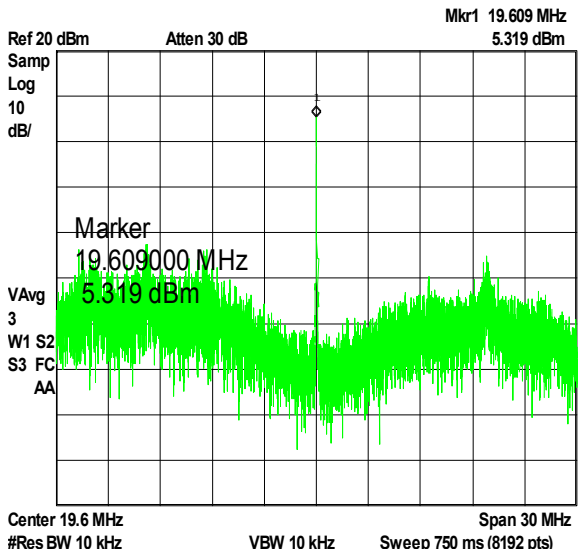


Figure 5.27 Measure output spectrum of the second-generation 2nd-order bandpass ΣΔM with a 19.6-MHz MEMs resonator

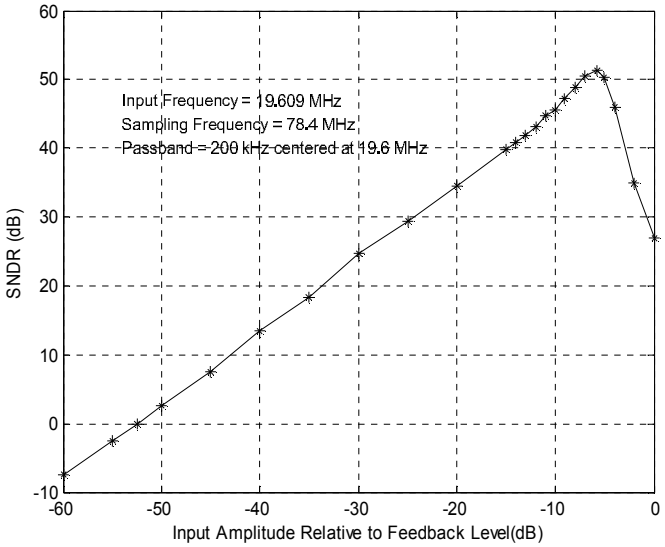


Figure 5.28 Measured SNDR plot of the ΣΔM tested with the MEMS resonator

Table 5.4 Performance summary of the ΣΔM employing MEMS resonator

Technology	0.35-μm CMOS
Supply Voltage	3.3 V
Power Consumption	28 mW
Active Chip Area	0.7×0.7 mm^2
Modulator Order	2
Filter type	MEMS
Sampling Frequency	78.4 MHz
Center Frequency	19.6 MHz
Bandwidth	200 kHz
OSR	196
Dynamic Range	52.5 dB
Peak SNDR	51 dB

power consumption is possible. The measured performance is summarized in Table 5.4.

5.3.4 Experimental Results of the 2nd-Generation 4th-Order Bandpass ΣΔM

The prototype 4th-order bandpass ΣΔM is tested with two 47.3-MHz off-chip SAW resonators. Figure 5.29 shows the measured output spectrum of the 4th-order bandpass ΣΔM. The measured peak SNDR and dynamic range in a 200-kHz bandwidth centered at 47.3MHz are 66dB and 69dB, respectively, as depicted in Figure 5.30. A similar

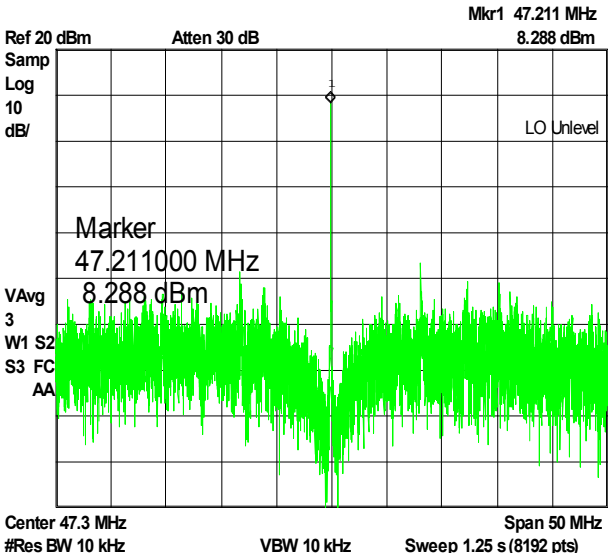


Figure 5.29 Measured output spectrum of the 4th-order bandpass ΣΔM with two 47.3-MHz SAW resonators

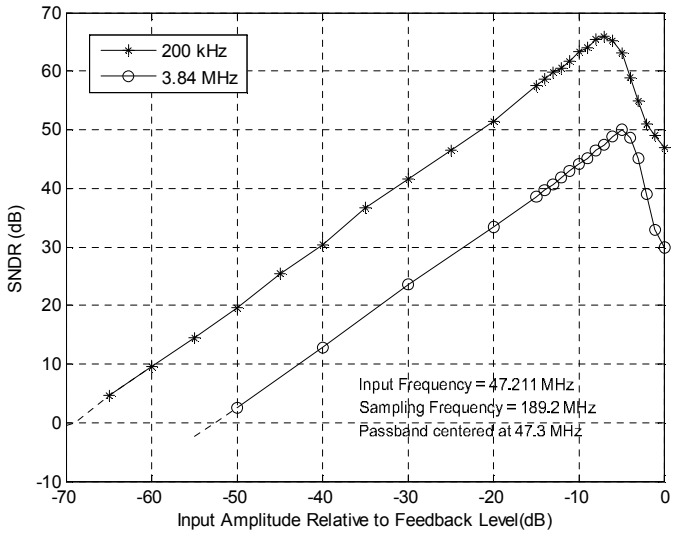


Figure 5.30 Measured SNDR plots of the 4th-order bandpass ΣΔM

comparison is made with some previously published CMOS/BiCMOS single-bit higher-order (>4) bandpass ΣΔMs and listed in Table 5.5. The measured SNDR and FOM in 200-kHz signal bandwidth is comparable with CT bandpass ΣΔMs and most of the DT bandpass ΣΔMs, but much lower than those in [14][15].

Table 5.5 Performance comparison of the 4th-order SAW resonator based bandpass ΣΔM with previously published work.

Design	**This Work**		[27]	[30]	[21]	[11]	[15]	
Technology	**0.35-μm CMOS**		0.5-μm CMOS	SiGe	0.25-μm CMOS	0.35-μm CMOS	0.35-μm CMOS	
Supply Voltage	**3.3V**		5V/3.3V	3V	1V	3.3V	3V	
Type	**SAW**		Opamp-RC	Gm-C	Swithced-Opamp	SC	SC	
Modulator Order	**4**		6	4	4	6	4	
Power	**45mW**		60mW	64mW	8.45mW	76mW	24mW	
Sampling Frequency	**189.2MHz**		40MHz	800MHz	7.13MHz	42.8MHz	80MHz	
Center Frequency	**47.3MHz**		10.7MHz	200MHz	10.7MHz	10.7MHz	20MHz	
Bandwidth	**200k**	**3.84M**	200kHz	200kHz	200kHz	200kHz	270k	3.84M
OSR	**473**	**24.6**	100	2000	35.65	107	148.15	10.42
Dynamic Range	**69dB**	**52.5dB**	67dB	N/A	62dB	74dB	86dB	50dB
Peak SNDR	**66dB**	**50dB**	63.5dB	68dB*	59.5dB	61dB	78dB	46dB
FOM	**132.48**	**129.31**	128.73	132.95	133.24	125.2	148.51	128.04

"*": denote only peak SNR performance reported

The measured SNDR of the 4th-order bandpass ΣΔM has significant degradation from that obtained in the post-layout simulation, i.e. 66dB cf. 78dB. Several effects could contribute to the SNDR degradation, such as clock jitter and noise. For this specific design employing two offchip SAW resonators, the mismatch between the two anti-resonance cancellations may also account for the performance degradation, since it is difficult to ensure that the anti-resonances of the two resonators are fully cancelled at the same time during the testing. Unlike in the simulation, the quality of the tuning in the experiment can only be observed through the overall output spectrum. Since there are two resonators involved, it is a two-dimensional tuning. It is not easy to cover the entire two-dimensional turning space with fine tuning steps and find the optimum cancellation. The effect of anti-resonance cancellation mismatch on the SNDR performance has been investigated in the simulation and shown in Figure 5.31. The equi-SNDR curves are

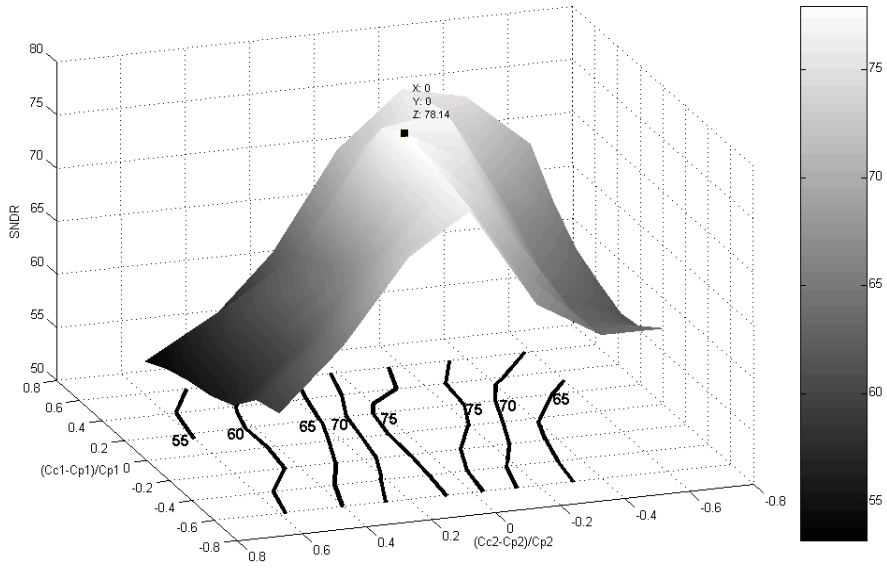


Figure 5.31 Effect of the cancellation mismatch in 4th-order bandpass ΣΔM

plotted on the X-Y plane. It can be seen the SNDR is quite sensitive to the mismatch between the two anti-resonance cancellations, especially to the anti-resonance cancellation of the second resonator. Better cancellation matching may be achieved by accurate modeling of the parasitic capacitance and on-chip cancellation. Other than the anti-resonance cancellation mismatch, the feedback coefficients variation during the measurement may also contribute to significant SNDR degradation. In spite of these problems, the measured performance for a 3.84-MHz signal band yields a peak SNDR of 50dB and dynamic range of 52.5dB, an effective 8-bit resolution which meets the requirement for WCDMA receivers.

CHAPTER 6

IMPLEMENTATION OF ELECTROMECHANICAL FILTER BASED CT BANDPASS ΣΔM

The design methodology and modulator architecture discussed in chapter 4 gives the possibility to realize CT bandpass ΣΔM employing single electromechanical filter, including LCRs SAW filter and mechanically-coupled MEMS filter. Such architecture is suitable for wideband ΣΔM by customizing the filter specification. Although MEMS filter is a favorable candidate since it is small in dimension and silicon compatible, it is not available at the time of this work. The circuit implementation described in this chapter is based on an off-shelf 110-MHz LCRs SAW filter with 1.1-MHz bandwidth.

6.1 Circuit-Level Architecture

The 4^{th}-order 110-MHz LCRs SAW filter based CT bandpass ΣΔM is implemented in a BiCMOS process with SiGe heterojunction bipolar transistor (HBT) and standard 0.35-μm CMOS. The HBT provided in the process has a peak unit current gain cutoff

Table 6.1 Design specifications

Technology	0.35-μm SiGe HBT BiCMOS
Supply Voltage	3 V
Type	LCRs SAW filter
Sampling	440 MHz (1 GHz maximum)
Center Frequency	110 MHz (250 MHz maximum)
Bandwidth	1 MHz
Modulator Order	4
Expected	11 bit (68dB)

frequency (f_T) of 50GHz. The adoption of this BiCMOS process makes it easy to meet the requirement of the high sampling frequency of 440MHz. In anticipating or acquiring filters with higher center frequency of 250MHz and sampling frequency of 1GHz, the 4^{th}-order ΣΔM is over-designed and can operate at sampling frequency of to 1GHz. The design specifications for the bandpass ΣΔM are listed in Table 6.1.

Figure 6.1 shows the simplified circuit-level architecture of the proposed CT bandpass ΣΔM employing LCRs SAW filter [137]. The input transconductor translates the input voltage signals to currents which is then subtracted from the properly weighted currents from RZ and HRZ DACs. Two pull-up resistors (R_{p1}=400Ω) to the power supply are used to provide the quiescent current at the current summation points and convert the signals from current to voltage in order to drive the offchip LCRs SAW filter. R_{p1} can not be too large due to high speed requirement and because it needs to drive offchip SAW filter. Note that even if only one single-ended signal is used to drive the offchip SAW filer, the other single-ended signal is also connected to a same pad so as to balance the signals at summation points and improve the linearity of the modulator. The single-ended output of the SAW filter is sensed by a low power wideband

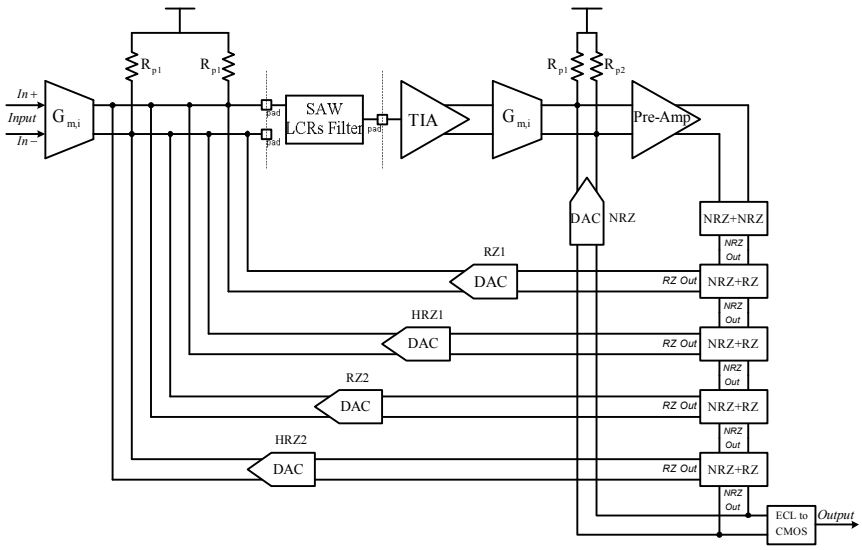


Figure 6.1 Circuit architecture of the LCRs SAW filter based bandpass ΣΔM

transimpedance amplifier (TIA) and converted back to differential signals. After that, the voltage signals are converted to currents and summed with the signal from the weighed NRZ DAC, and converted back to voltages by two pull-up resistors. Amplified further by a pre-amplifier, the summation signal is fed to five serially-connected ECL master-slave latches. Together with the pre-amplifier, the first master-slave latch, in which both master and slave stages have NRZ outputs, serves as the quantizer (comparator) in the ΣΔM and provides a half sampling cycle delay. The following four master-slave latches are serially connected by the NRZ master stages and the outputs of their slave RZ stages are used as control signals for the feedback current steering DACs. The differential ECL output of NRZ stage in the last latch is converted to single-ended CMOS logic level before driving the CMOS digital output pad.

6.2 Circuit Blocks

In this section, the detailed design of each major circuit block is covered, which includes input transconductor, TIA, master-slave latches, clock generation circuit, DAC and ECL to CMOS converter.

6.2.1 Input Transconductor

The input transconductor should have wide bandwidth, high linearity and low noise. Moreover, the transconductor also needs to drive two pull-up resistive loads (R_{p1}). Therefore, a BiCMOS transconductor based on the simple differential pair with emitter degeneration is adopted. To improve the linearity and input range of the transconductor without using large bias current, an extra pair of negative feedback auxiliary amplifiers (Q1,2 and Q3,4) is placed around the differential pair. Figure 6.2 shows the schematic the transconductor. All the inputs devices are SiGe HBTs because of their high transconductance. MOS devices are used for the tail and active-load transistors since

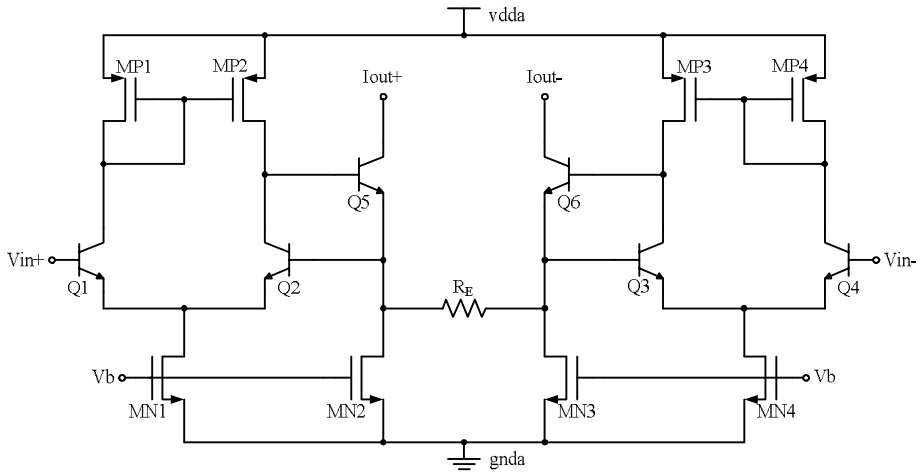


Figure 6.2 Schematic of the input transconductor

they are easy to bias and can achieve large small-signal output resistance, and large gain at small silicon area. Note that no common-mode feedback circuit is needed, since the resistive loads (R_{pl} in Figure 6.1) provide reasonable stable common-mode output.

Considering that if the auxiliary amplifiers are not used and V_{be} voltages of Q5 and Q6 are assumed to be constant, the emitter currents I_{EQ5} and I_{EQ6} are independent on V_{be} and given by

$$\begin{cases} I_{EQ5} = I_{MN2,3} + \dfrac{v_{in}}{R_E} \\ I_{EQ6} = I_{MN2,3} - \dfrac{v_{in}}{R_E} \end{cases} \tag{6.1}$$

where $I_{MN2,3}$ is the bias current and v_{in} is the differential input voltage. The differential output current is

$$i_o = \frac{v_{in}}{R_E} \tag{6.2}$$

if the base currents of Q5 and Q6 are ignored. Then the transconductance of this simple emitter degenerated transconductor is calculated by

$$G_m = \frac{1}{R_E} \tag{6.3}$$

However, the V_{be} is not ideally constant. The dependency of emitter current I_E on V_{be} is reflected by the small signal emitter resistance,

$$r_e = \frac{\partial V_{be}}{\partial I_E} = \frac{V_T}{I_E} \tag{6.4}$$

The varying V_{be} voltage will make the differential output current being a significant non-linear function of the input voltage and introduce large distortion. The overall transconductance with variation of V_{be} in consideration can be calculated by small signal analysis and given by

$$G_m = \frac{1}{2r_e + R_E} \tag{6.5}$$

Thus r_e should be kept small compared with R_E to obtain high linearity. This requires that the bias current should be large and the input signal should be kept small. The reduced input signal will affect the dynamic range of overall ΣΔM.

By introducing the auxiliary amplifiers, the negative feedback configurations of the amplifiers force the emitter voltages of Q5 and Q6 to be equal to those of Vin+ and Vin-. As a result, the input voltage acts on R_E directly and does not depends on the V_{be} of Q5 and Q6 and the overall transconductance is almost solely dependent on the inverse of R_E. The linearity and input range of the modified transconductor are significantly improved. It can be shown that the input-referred noise density of the transconductor is dominated by the current sources (MN2/3), R_E and pull up resistors R_{p1} given in Figure 6.1. Taking only the thermal noise in consideration, the input-referred noise is approximate by

$$V_{n\_Gm}^2 = 4kT\left(\frac{\gamma}{2} g_{m\_MN2/3} R_E^2 + R_E + 2\frac{R_E^2}{R_{p1}}\right) \tag{6.6}$$

Small R_E is preferred for low noise requirement, but may deteriorate the linearity of the transconductor. Given R_{p1}=400Ω, R_E is chosen to be 2kΩ to maintain good linearity and achieve reasonable low noise. According to (6.6), noises coming from pull-up resistors

become dominant. The simulated in-band noise of the transconductor is about 85dB lower than full-scale input signal FS=500mV$_{pp}$. The realized transconductor can operate up to gigahertz range with good linearity at moderate current consumption (~2mA). IM3 better than 80dB can be achieved in post-layout simulation with two tones test (-12dBFS).

6.2.2 Low Power Wideband TIA

As discussed in chapter 4, to make the phase delay negligible, a bandwidth of at least 10 times of the 110-MHz center frequency is need for the TIA, which senses the output of LCRs SAW filter and provides at least 30-dB voltage gain. A straightforward implementation of such wideband TIA consumes too much power, given large parasitic capacitance (C_p=5~8pF) at its input. This defeats the purpose of using the passive electromechanical filter. In this work, emitter peaking technique is used to design wideband TIA with reasonable low power consumption. The schematic of the proposed TIA is shown in Figure 6.3. The circuit on the left side is the core transimpedance

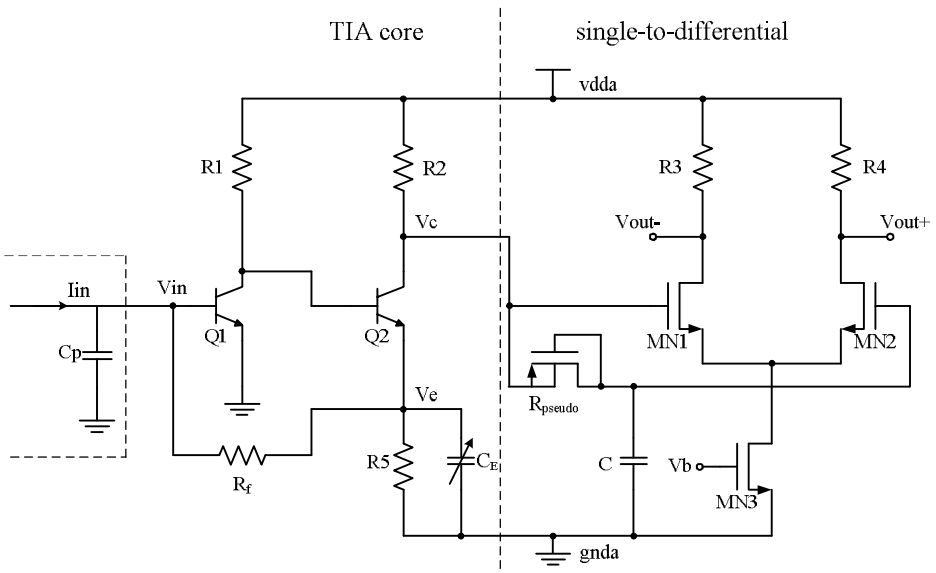


Figure 6.3 Schematic of the proposed TIA

amplifier; the remaining circuit on right side forms a single-ended to differential converter.

The design of the core transimpedance amplifier is based on the traditional two-stage amplifier with shunt-series feedback. The shunt-series feedback topology is chosen over the shunt-shunt one (that is, the output is taken at emitter of Q2) for the following two reasons. First, the DC level at the output is close to power supply which facilitates the design of subsequent single-ended to differential converter stage. Second, the feedback signal is isolated from the input capacitance of the subsequent stage. To achieve wide bandwidth at low power consumption, a peaking capacitor C_E is added at the emitter of Q2. The inclusion of this peak capacitor enhances the bandwidth of the proposed TIA, which is explained as follows.

If no peaking capacitor is introduced, the transfer function of the core TIA can be well approximated by a first-order function,

$$\frac{V_c}{I_{in}} = \frac{A_0 R_f}{A_0 + 1} \cdot \frac{R_2}{R_5 // R_f} \cdot \frac{1}{1 + \frac{R_f C_p}{A_0 + 1} s} \tag{6.7}$$

where C_p (5~8pF) is the total parasitic capacitance at the input of the TIA, as discussed in chapter 4. Since the 3-dB bandwidth of open-loop amplifier can be much larger than the inverse of the time constant $R_fC_p/(A_0+1)$, its transfer function is only approximated by its DC gain A_0 ($\approx g_{m\_Q1}R_1$). Therefore, the overall close-loop amplifier provides a transimpedance gain of approximately R_f, and with a 3-dB bandwidth equal to

$$\omega_{-3dB} = \frac{A_0 + 1}{R_f C_{in}} \approx \frac{A_0}{R_f C_{in}} \tag{6.8}$$

and the input resistance is

$$R_{in} \approx \frac{R_f}{A_0} \tag{6.9}$$

After adding the peaking capacitor C_E, a dominant pole close to (6.6) is introduced and the transfer function of open loop amplifier is given by

$$A(s) = \frac{A_0}{1 + \frac{s}{\omega_{p1}}} \tag{6.10}$$

where ω_{p1} is approximated by

$$\omega_{p1} \approx \frac{g_{m\_Q2}}{C_E} \tag{6.11}$$

Therefore, the close loop transfer function is re-calculated as

$$\begin{aligned} \frac{V_c}{I_{in}} &= \frac{A_0\omega_{p1}/C_p}{s^2 + \frac{R_fC_p + 1/\omega_{p1}}{R_fC_p/\omega_{p1}}s + \frac{(A_0+1)\omega_{p1}}{R_fC_p}} \cdot \frac{R_2}{R_5 // R_f} \cdot \left(1 + \frac{s}{1/(R_5 // R_f)C_E}\right) \\ &= \frac{A_0R_f}{A_0+1} \cdot \frac{R_2}{R_5 // R_f} \cdot \left(1 + \frac{s}{1/(R_5 // R_f)C_E}\right) \cdot \frac{\omega_n^2}{s^2 + \frac{\omega_n}{Q}s + \omega_n^2} \end{aligned} \tag{6.12}$$

where

$$\omega_n = \sqrt{\frac{(A_0+1)\omega_{p1}}{R_fC_p}} \tag{6.13}$$

and

$$Q = \frac{\sqrt{(A_0+1)R_fC_p\omega_{p1}}}{R_fC_p\omega_{p1} + 1} \tag{6.14}$$

First, we consider the effect of poles in (6.12). They are complex conjugate if Q>0.5, and then the bandwidth can be broadened due to cancellation of imaginary parts. An insight evaluation of (6.12) indicates that the maximum bandwidth can be obtained when $Q=\sqrt{2}/2$, that is

$$\omega_{-3dB} = \omega_n\big|_{Q=\sqrt{2}/2} \approx \frac{\sqrt{2}A_0}{R_fC_{in}} \tag{6.15}$$

Compared with (6.8), the bandwidth is improved by about 41%. When $Q>\sqrt{2}/2$, the step response exhibits ringing. Generally speaking, Q can be changed from 0.5 to 1 in practical design. Moreover, according to (6.12), C_E also introduces a zero, which can be adjusted to be near passband and is used to broaden the bandwidth further. C_E is implemented by a 4-bit programmable capacitor bank.

As to the single-ended to differential converter, a RC lowpass filter is used to extract the DC level of V_c and apply the DC voltage to one of the inputs of the following differential pair. The lowpass filter needs to be designed with very low cutoff frequency. This means constituent resistor and capacitor with very large values are needed. It is undesirable to realize them both with on-chip integrated passive device because of their large silicon areas occupation. A MOS-bipolar device is used as a pseudo-resistor [138], because for small voltage across the device, its incremental resistance is extremely high. Therefore, a reasonable size (7pF) on-chip capacitor can be used and much silicon areas can be saved.

The simulated frequency responses in post-layout level of the TIA with/without C_E=0.8pF are shown in Figure 6.4 (with the single-ended to differential converter

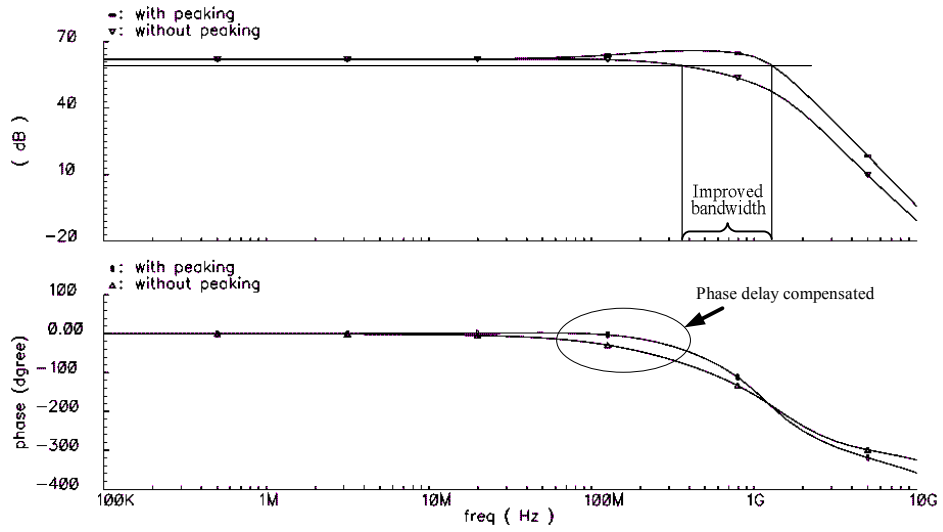


Figure 6.4 Simulated frequency response of TIA with/without peaking capacitor

included). The TIA has an input resistance of 25Ω, transresistance of 62dBΩ (equivalent 34-dB voltage gain). The 3-dB bandwidth is improved from 360MHz to 1.3GHz with the aid of peaking capacitor at only 2-mA current consumption and the phase delay in the vicinity of 110-MHz center frequency is negligible.

6.2.3 Comparator and Latches

As introduced in section 6.1, the BiCMOS comparator consists of a preamplifier and a modified ECL master-slave latch with NRZ output. The circuit schematics of the preamplifier and latch are shown in Figure 6.5 and Figure 6.6, respectively. The preamplifier needs to provide about 20-dB gain, thereby lowering the offset contributed by the latch and alleviating metastability problem. It also helps suppress the kickback noise generated by the latch to an acceptable level. Moreover, to avoid introducing excess phase delay in the forward path of the ΣΔM, a wide bandwidth is also preferred. The pre-amplifier achieves 20-dB gain and more than 2.5-GHz bandwidth in post-layout simulation at only 1-mA current consumption. The ECL master-slave latch used is

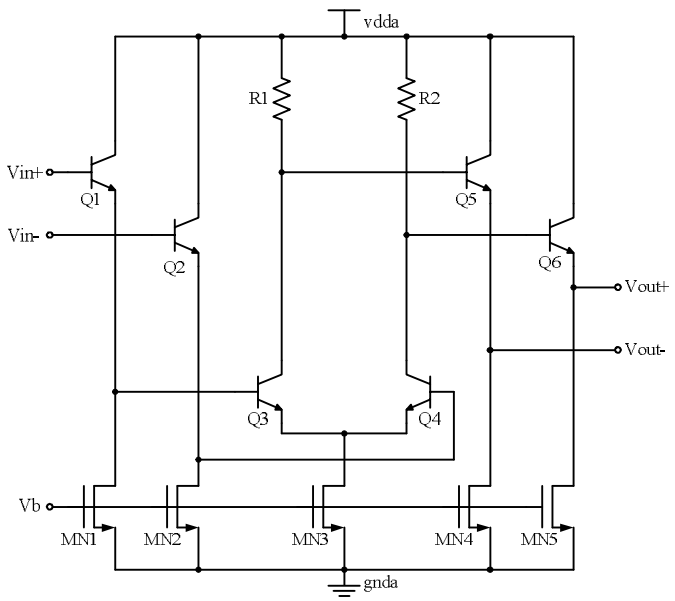


Figure 6.5 Schematic of the pre-amplifier

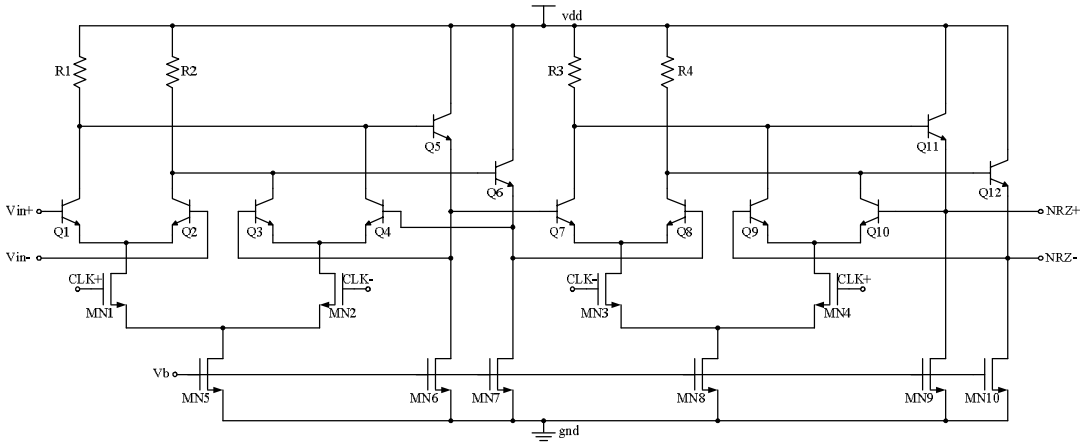


Figure 6.6 Schematic of the ECL master-slave latch with NRZ outputs

modified from a classical bipolar master-slave latch by replacing its latching transistors with NMOS devices. The use of NMOS as latching transistors means that the net load on the clock driver is mainly capacitive. This simplifies the design of clock driver (CMOS logic) and save the chip area. Although the operating speed may suffer a little, the latch still can be clocked up to 1GHz.

The remaining four latches, as shown in Figure 6.7, are realized using slightly different circuit to generate the control signals for RZ and HRZ DACs with proper delay. By diode-connecting the final differential pair (Q9 and Q10) rather than cross-coupling

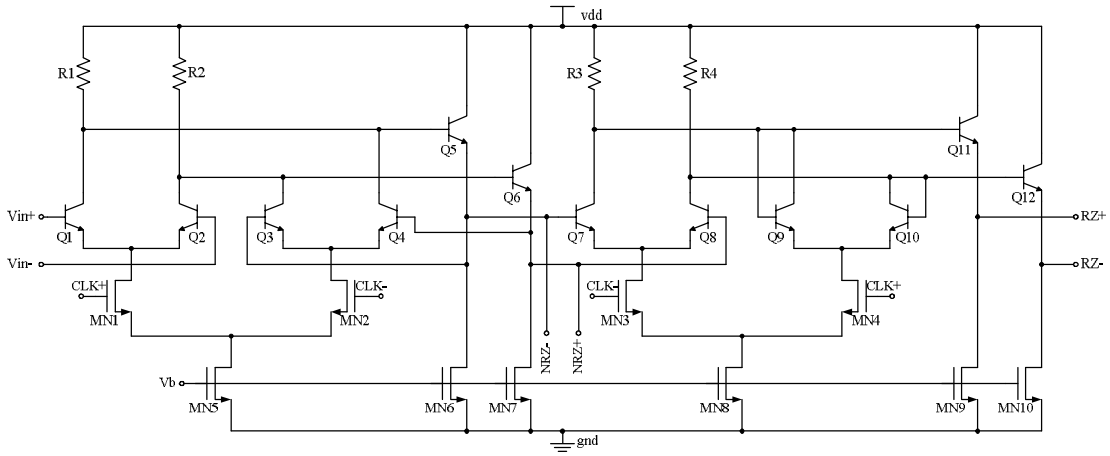


Figure 6.7 Schematic of the ECL latch with NRZ master output and RZ slave output

them, an master-slave latch with NRZ output at master stage and RZ output at slave stage can be easily realized [139]. This type of latch is used for the next four serially-connected latches after the main comparator to generate the control signals for RZ and HRZ DACs with proper delays.

6.2.4 Clock Driver

If for a period of time, both MN1 and MN2 in master latch (or MN3 and MN4 in slave latch) in Figure 6.6/6.7 are turned off, the voltage levels of their source nodes will drop significantly and rise back to their normal values when one of the transistors is turned on. This causes the fluctuation of current in the current source MN5 and results in glitches at the outputs of the latch. The resultant glitches can cause large kickback noise to the latch inputs. Moreover, they may also affect the settling time of the feedback current steering DACs if such latch outputs are used to control the DACs.

To avoid this problem, a high cross clock signal can be used to drive the latch to prevent MN1 and MN2 (or MN3 and MN4) from turning off simultaneously. Figure 6.8 shows the high-cross clock generator and driver which consists of a high-cross generator, MN1-2 and MP1-2, and a variable-delay inverter chain that drives the NMOS latching

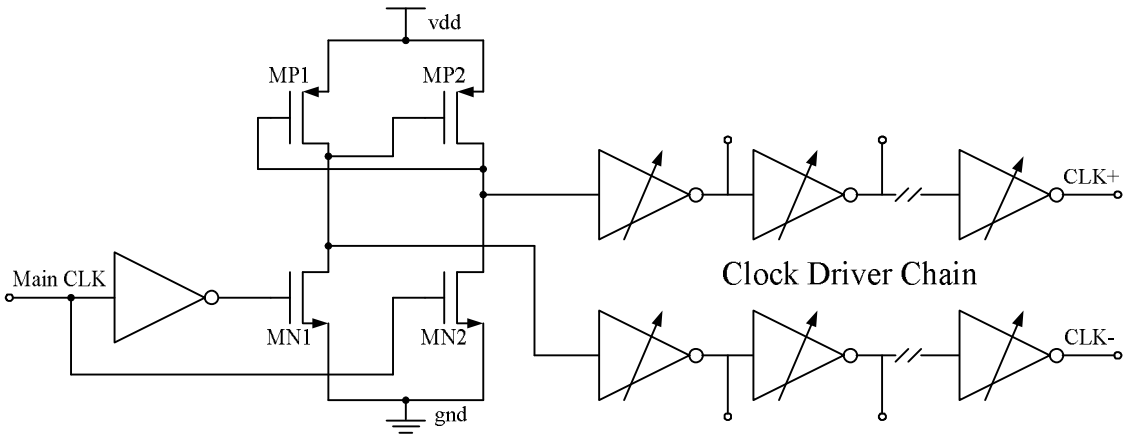


Figure 6.8 Schematic of the clock driver

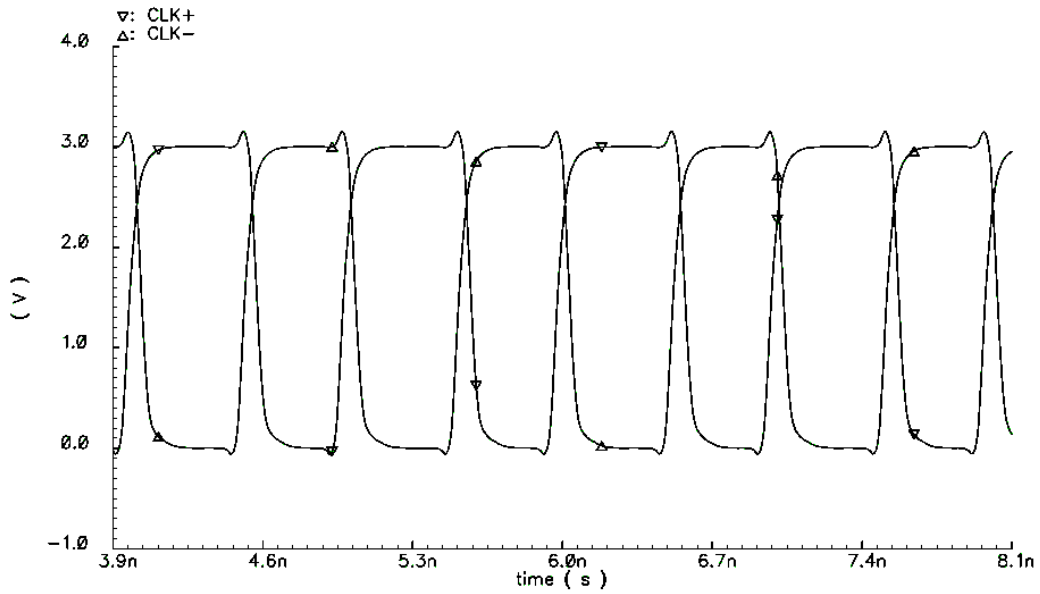


Figure 6.9 Simulated outputs of the high-cross clock driver

transistors in the master-slave latches. The simulated outputs of this clock driver are given in Figure 6-9.

To reduce the clock jitter due to the on-chip devices, which is mainly determined by power supply and substrate noise, separated power supply pins are assigned to the clock driver and on-chip decoupling is used.

6.2.5 Current Steering DACs

Five current steering DACs are implemented by cross-coupled current steering differential-pairs, as shown in Figure 6.10. Simple current steering differential pairs, which are frequently adopted in high speed DAC design, are not used here because they are sensitive to the imperfection of input signals. In the cross-couple differential pairs, the spikes and ripples at the input of the DACs can be better rejected. The feedback back coefficient associated with the DAC is determined by the difference between the two tail currents, $I_{ref}+I_{DAC}$ and $I_{ref}-I_{DAC}$. I_{ref} denotes the static current if both inputs of the DAC are turned on and I_{DAC} is directly scaled by the feedback coefficients.

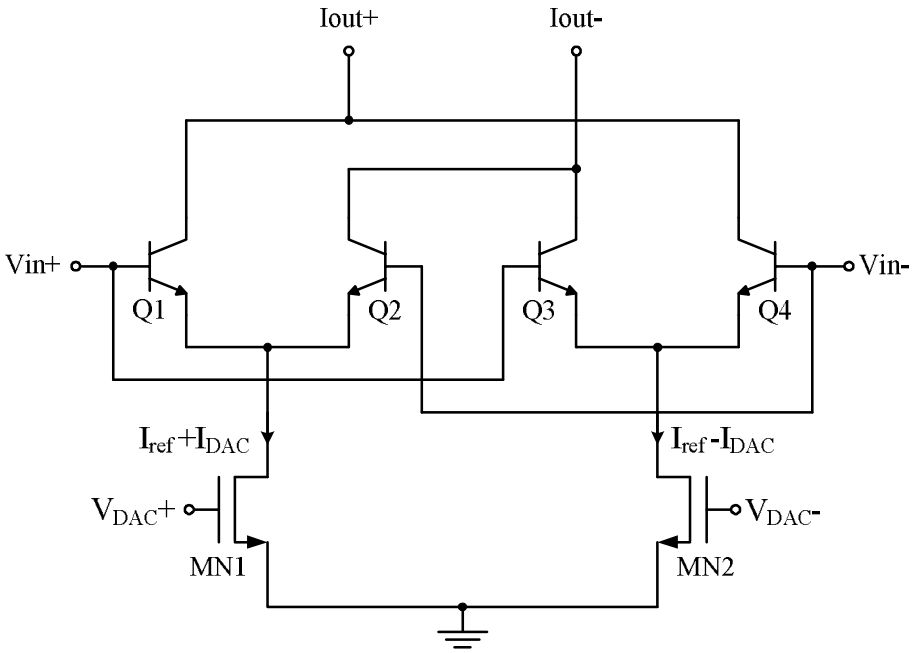


Figure 6.10 Schematic of the current steering DAC

The input-referred noise of the ΣΔM due to the DAC is dominated by two current sources MN1 and MN2, and given by

$$V_{n\_DAC}^2 = 4kT\gamma\left(g_{m\_MN1} + g_{m\_MN2}\right)R_E^2 \tag{6.16}$$

A noise simulation in post-layout level for the entire 4th-order bandpass ΣΔM indicates that SNR considering only device noise is 83dB in 1-MHz bandwidth. About 70% input referred noise is from the pull-up resistors, as discussed in section 6.2.1.

6.2.6 ECL-to-CMOS Converter

As depicted in Figure 6.1, the NRZ output of the master stage of the last master-slave latch is still in ECL logic level (350mV for single-ended and 700mV for differential output). To interface with the CMOS output pad provided by the foundry, an ECL-to-CMOS converter is needed. Figure 6.11 shows the schematic of a modified current mirror based ECL-to-CMOS level converter.

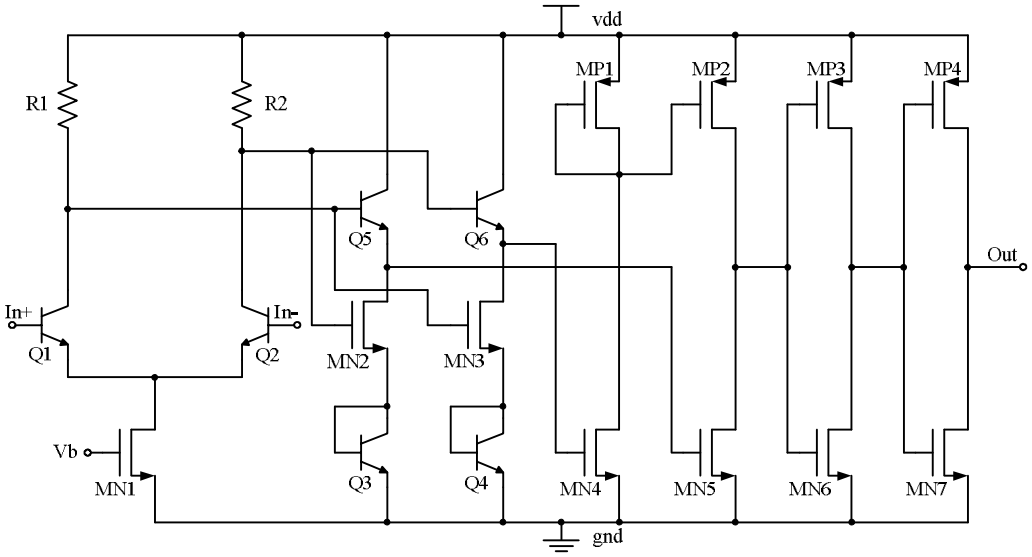


Figure 6.11 Schematic of the ECL-to-CMOS converter

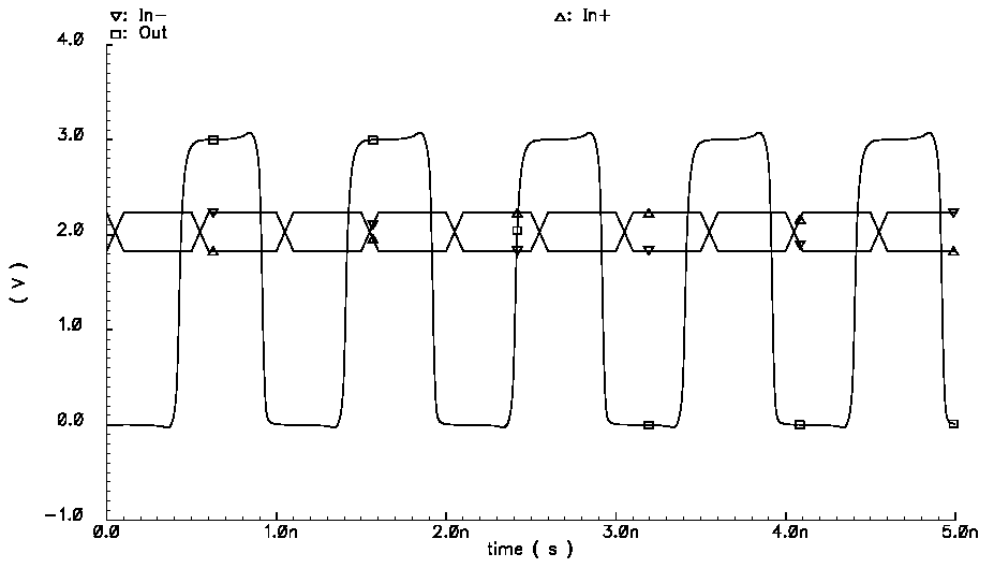


Figure 6.12 Simulated transient response of the ECL-to-CMOS converter

The operation of this circuit is quite simple. The 700-mV swing differential ECL inputs are firstly amplified by the input differential pair to about 2V. After level-shifted down by a couple of emitter followers, they are further amplified and converted to a single-ended signal with swing closer to CMOS level by NMOS pair MN4 and MN5 with a PMOS current mirror load. More than one CMOS inverters are used as output buffers to further amplify the signal to full-swing CMOS level. The simulated input and

output signals of the designed ECL-to-CMOS converter at 1GHz are shown in Figure 6.12. The ECL input is converted to CMOS output with some delay.

6.3 Experimental Results

The proposed 110-MHz LCRs SAW filter based CT bandpass ΣΔM is implemented in a 0.35-μm SiGe HBT BiCMOS process and operates from 3-V supply voltage. Figure 6.13 shows the chip micrograph, which has a die size of 0.67×0.83 mm^2 excluding pads. The main circuit blocks are identified.

The fabricated chip (DUT) is mounted in a 44-pins ceramic quad flat pack (CQFP) and soldered directly onto a double-layer testing PCB. In order to reduce the wiring parasitic, the SAW filter is placed as close as possible to the DUT. Separated voltage regulators are used to minimize the crosstalk among different power supplies such as

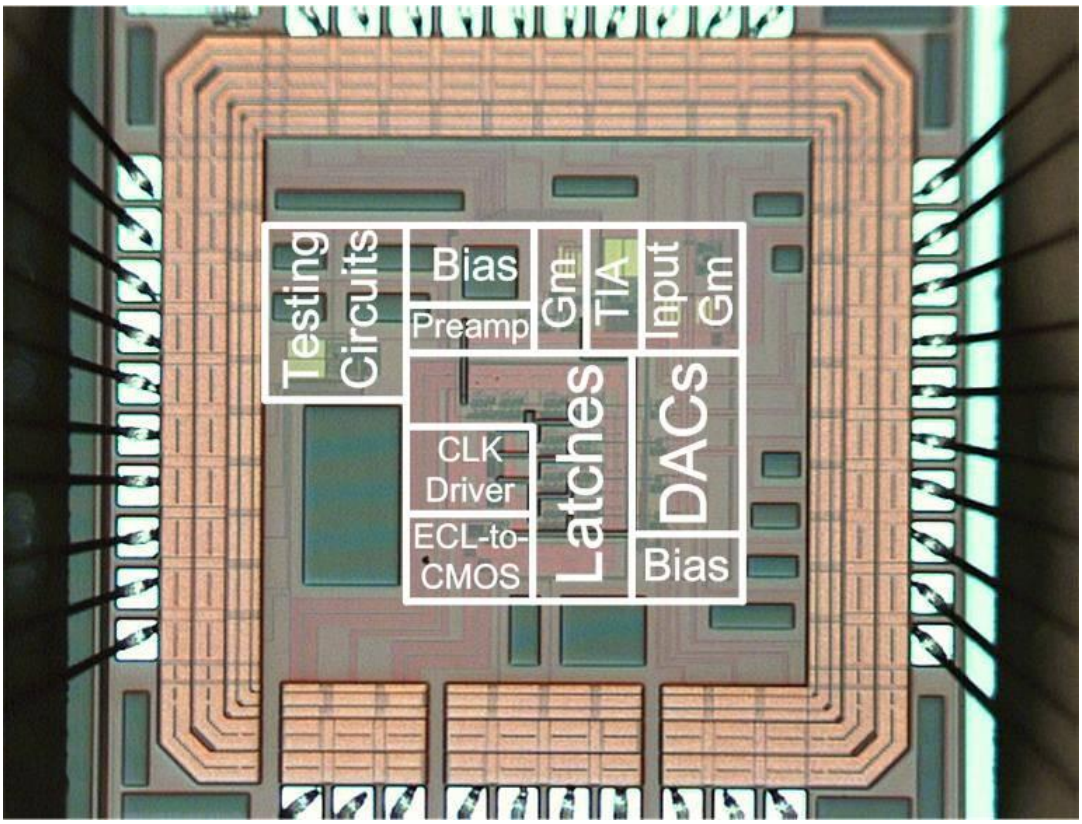
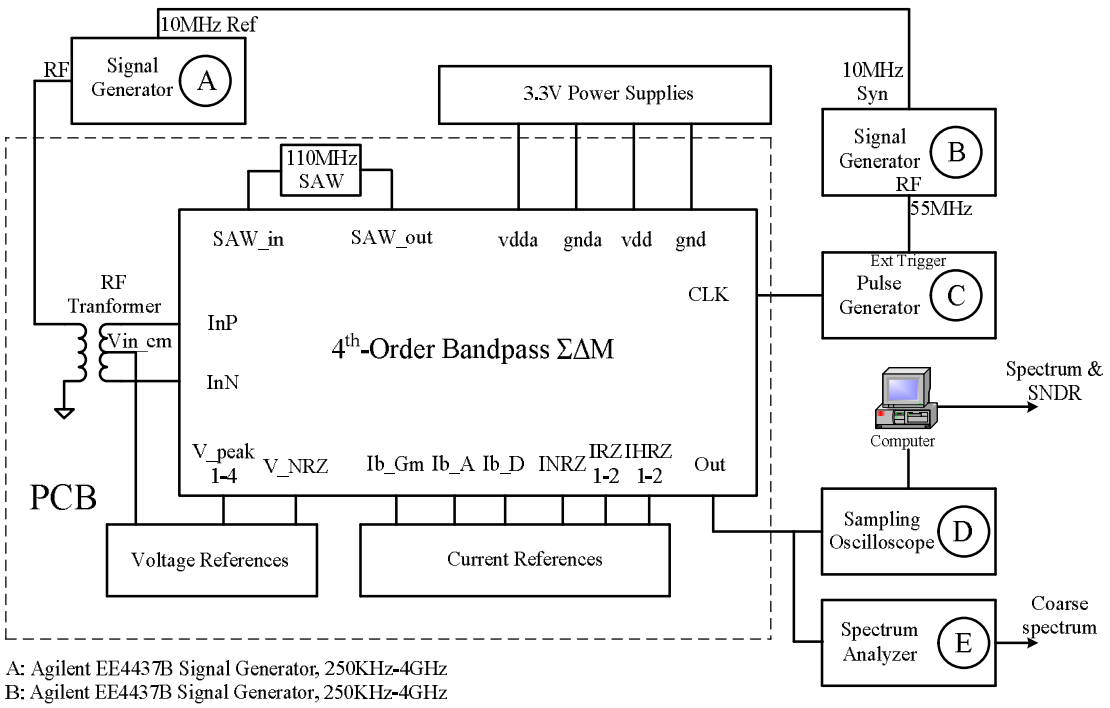


Figure 6.13 Microphotograph of the SAW filter based bandpass ΣΔM chip

analog supply vdda, digital supply vdd, supply for clock driver and supply for the peripheral devices on board. Decoupling capacitors are extensively used and placed close to the voltage regulators and mounted chip.

Figure 6.14 shows the measurement setup of the 4th-order bandpass ΣΔM tested with 110-MHz LCRs SAW filter. The ΣΔM is clock at 440MHz by an external pulse generator, and the output signal is firstly fed to a spectrum analyzer to observe a rough output spectrum and verify its function. As already mentioned in last chapter, spectrum analyzer is not the best way to characterize the performance of a ΣΔM accurately, especially when the clock speed exceeds several hundred megahertz. In high frequency operation, the spectrum analyzer becomes more sensitive to the analog imperfections in the output bit stream, such as noise and rising/falling edge asymmetry of bit stream which are mainly caused by the output buffer. Therefore, the output is also captured



A: Agilent EE4437B Signal Generator, 250KHz-4GHz
B: Agilent EE4437B Signal Generator, 250KHz-4GHz
C: Agilent 8133A Pulse Generator, 3GHz
D: Agilent Infiniium DSO80604B Sampling Oscilloscope, 6GHz, 40GSa/s
E: Agilent E4407B Spectrum Analyzer, 9KHz-26.5GHz

Figure 6.14 Test setup of the SAW filter based 4th-order bandpass ΣΔM

asynchronously at 4GSa/s by an advanced high speed oscilloscope (40GSa/s maximum, 4-MSa memory depth). Since the captured output data is oversampled asynchronously, the true bit stream (440MSa/s) must be reconstructed. This can be accomplished by interpolating the captured samples, and then recovering timing from the reconstructed eye diagram. The resultant data is filtered and decimated to extract the 440-MSa/s bit stream. A 65536-point windowed FFT is then performed to obtain the output spectrum from which the SNDR is calculated. To further improve the accuracy, the pulse generator is externally triggered by a low phase noise signal generator (at 55MHz) locked to the 10-MHz reference of the low phase signal generator which provides input signal for the bandpass ΣΔM under test.

Figure 6.15 shows the output spectrum of the bandpass ΣΔM when the reconstruction is not applied. The noise floor level is greatly affected by the bit stream's noise. Noise shaping can not be observed even in 10-MHz view of bandwidth, as shown in Figure 6.15(b). The peak SNDR performance is only 40dB in 1-MHz signal bandwidth, which is quite closed to the value measured directly with the spectrum analyzer. After the data reconstruction, the output spectrum is greatly improved and the

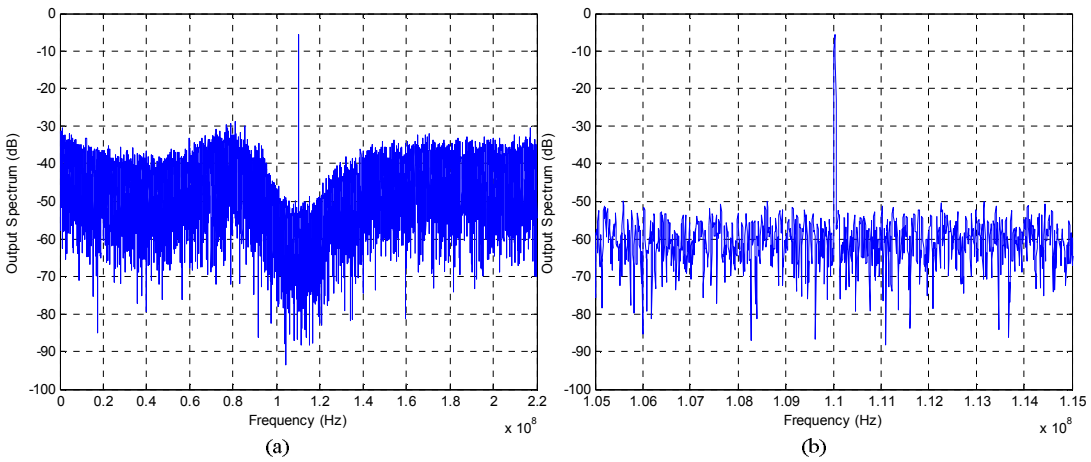


Figure 6.15 Measured output spectrum before data reconstruction

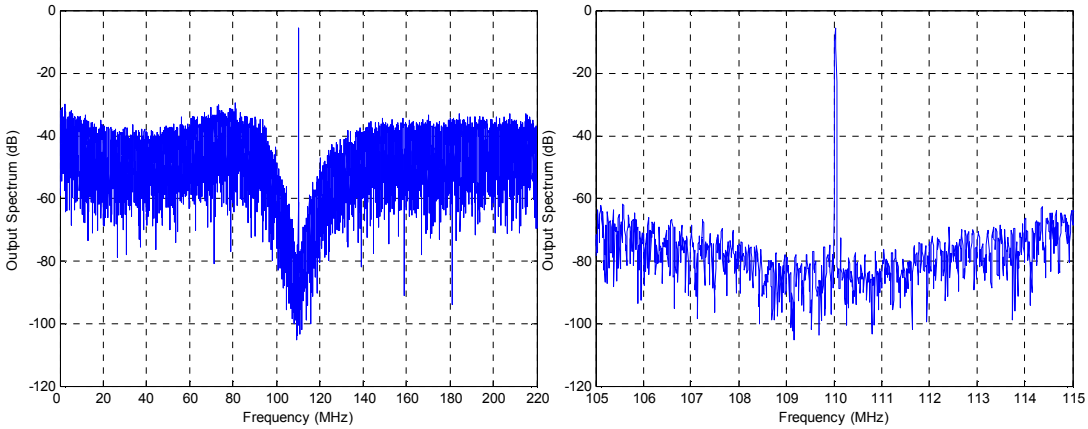


Figure 6.16 Measured output spectrum after data reconstruction

resultant spectrums are shown in Figure 6.16. This time, the noise shaping is well observed in the same 10-MHz bandwidth. Note that the width of frequency bins is approximately 6.7kHz. The measured peak SNDR and DR performances in 1-MHz signal bandwidth are 60dB and 65dB, respectively, as depicted in Figure 6.17. Compared with the 74-dB SNDR predicted by post-layout simulations, there is 14-dB degradation. This may be attributed to the approximation in the transfer function of the LCRs SAW filter. The clock jitter noise discussed in section 4.3.2 and the feedback coefficients variation during the measurement may also account for the degradation. The dynamic range in 3.84-MHz signal band is 58dB, also given in Figure 6.17. The power consumption is 57mW, excluding the output buffers. This relatively high power is due to the over-design mentioned in Section 6.1.

A two-tone intermodulation test is also performed to evaluate the linearity of the designed LCRs SAW filter based bandpass ΣΔM. Two sinusoidal signals with frequency separation of 400kHz and -14dBFS (f_1=110.029MHz and f_2=110.429MHz) are used to test the ΣΔM. The measured IM3 is about -52dBc, as shown in Figure 6.18. The single-ended interface circuits with the LCRs SAW filter and large signal dependent-parasitic

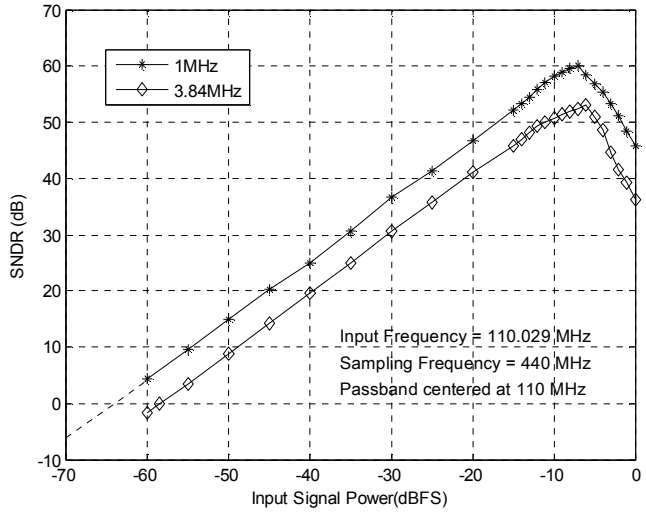


Figure 6.17 Measured SNDR versus input power

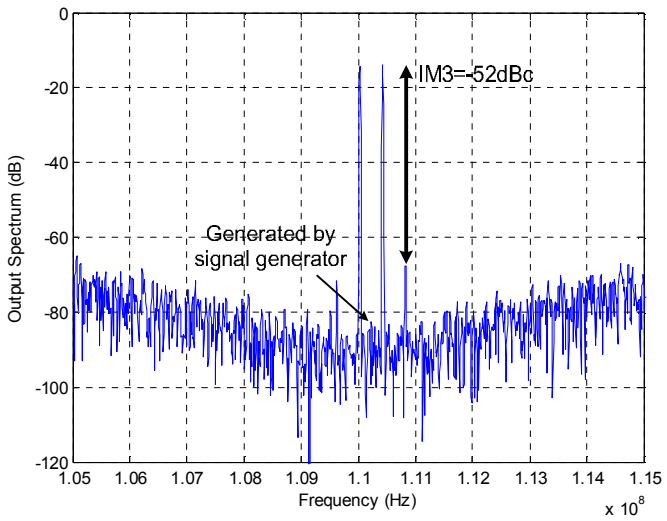


Figure 6.18 Two-tone test result

resulting from the externally connected SAW filter may account for the relatively poor linearity.

The measured performance is summarized in Table 6.1 and compared with some published CMOS/BiCMOS single-bit bandpass ΣΔMs with wideband (>1MHz) performance reported. The 110-MHz LCRs SAW filter based 4th-order bandpass ΣΔM has also achieved comparable FOM.

Table 6.2 Performance comparison of the LCR SAW filter based bandpass ΣΔM with previously published designs

Design	**This work**	[30]	[15]	[16]
Technology (μm)	**0.35/SiGe BiCMOS**	SiGe	0.35/ CMOS	0.35/ CMOS
SupplyVoltage (V)	**3**	3	3	3.3
Type	**SAW LCRs**	Gm-C	SC/sub-sampling	SC/double sampling
Modulator Order	**4**	4	4	2
Power (mW)	**57**	64	38	37
Sampling Frequency (MHz)	**440**	800	80	120
Center Frequency (MHz)	**110**	200	20 (60*)	60
Bandwidth (MHz)	**1/3.84**	1.97	3.84	1/1.25
OSR	**220/57.3**	203	10.42	120/96
Dynamic Range (dB)	**65/58**	56	50	N/A
Peak SNDR (dB)	**60/53**	58	46	55/52
FOM	**132.4/131.3**	132.9	128	129.3/127.3

"*" denote input frequency

The successful implementation of this work opens the possibility of realizing high performance bandpass ΣΔMs employing electromechanical filters. Low power implementation can be expected for future design, such as the CT bandpass ΣΔM with circuits and MEMS filter integrated on the same silicon substrate.

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

7.1 General Conclusions

The primary goal of this thesis is to investigate the feasibility of electromechanical resonator/filter based single-bit bandpass ΣΔM. The electromechanical resonator/filter is proposed to replace conventional electronic loop filters in the CT bandpass ΣΔMs, in order to overcome some of their drawbacks, such as low Q factor and the need of frequency tuning. The targeted applications are IF and any other bandpass digitization.

Since the electromechanical resonator/filter is non-ideal, the straightforward replacement will not result in functional bandpass ΣΔM. Several techniques have been proposed in this thesis to overcome the inherent non-idealities of the electromechanical resonator/filter, which include the anti-resonance in the electromechanical resonator, insertion loss in both resonator and filter, and the excess phase delay in the forward path of the ΣΔM. The anti-resonance in the resonator caused by the static capacitance is cancelled by the proposed cancellation technique based on negative capacitance, resulting in a near ideal resonator transfer function. The insertion loss is compensated by a gain stage with a separate or built-in phase regulator to neutralize the phase delay in the forward path and stabilize the ΣΔM.

With the above proposed techniques, the concept of electromechanical resonator/filter based bandpass ΣΔMs has been demonstrated in several prototypes realized in a 0.35-μm CMOS/BiCMOS technology. These include two generations of

SAW/MEMS resonators based 2nd-order bandpass ΣΔMs and a 4th-order SAW resonator based ΣΔM for narrowband digitization, and a 4th-order SAW filter based wideband bandpass ΣΔM.

The 2nd-order 47.3-MHz SAW resonator based ΣΔM has achieved a peak SNDR of 57dB in 200-kHz bandwidth, which is better than the previously reported conventional DT or CT 2nd-order bandpass ΣΔMs. The 2nd-order 19.6-MHz MEMS resonator based ΣΔM has a measured peak SNDR of 54dB, comparable with the conventional ones. A 4th-order 47.3-MHz SAW resonators based bandpass ΣΔM has also been demonstrated and obtained a measured SNDR of 66dB in 200-kHz signal bandwidth, which is about 12dB less than the simulation result. The mismatch between two anti-resonance cancellation circuits may account for this degradation.

Mechanically-couple MEMs and longitudinally-coupled SAW filters have been proposed to realize wideband bandpass ΣΔMs. A 4th-order bandpass ΣΔM employing a single 110-MHz SAW filter has been realized in a 0.35-μm SiGe BiCMOS process. It achieves a peak SNDR of 60dB and a DR of 65dB in 1-MHz bandwidth, a performance comparable with the previously published conventional ones.

The significance of the work in this thesis is that it has proved the feasibility of realizing high-speed bandpass ΣΔMs using electromechanical resonators/filters in CMOS/BiCMOS process and shown the potential to achieve high performance at low power consumption.

7.2 Original Contributions

The original contributions of this work are summarized as follows.

- An anti-resonance cancellation technique to cancel the anti-resonance in SAW/MEMS resonator.

- A phase compensation technique in the forward path to compensate the phase delay introduced by the gain stage and to maintain the stability of the ΣΔM.
- 2^{nd}- and 4^{th}-order 47.3-MHz SAW resonators based bandpass ΣΔMs in 0.35-μm CMOS process.
- A 2^{nd}-order 19.6-MHz MEMS resonator based bandpass ΣΔMs in 0.35-μm CMOS process.
- The architecture of the bandpass ΣΔM employing a single electromechanical filter, such as mechanically-coupled MEMS filter and longitudinally-coupled SAW filter.
- A 4^{th}-order 110-MHz 1-MHz bandwidth bandpass ΣΔM employing a 110-MHz SAW filter in 0.35-μm SiGe BiCMOS process.
- A low power wideband transimpedance amplifier employing shunt-series feedback and emitter peaking capacitance.

7.3 Future Work

The future work may focus on the following areas.

- The present anti-resonance is off-chip and tuned manually. This is not suitable for practical application. Robust anti-resonance cancellation may be achieved through accurate modeling of static capacitance and adaptive on-chip anti-resonance cancellation.
- Phase compensation is also adjusted manually in this thesis. More robust automatic compensation is preferred. An alternative approach is to minimize the phase delay (maximize the bandwidth) of amplifier after the electromechanical resonator/filter.

- Since electromechanical resonators/filters are essentially passive and consume little power. Therefore, they are good candidates for the low power bandpass ΣΔMs and may be further studied.
- A much wideband electromechanical filter based bandpass ΣΔM may be developed for the potential applications in multi-band wireless receivers.

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APPENDIX A LIST OF PUBLICATIONS

[1] R. Yu and Y.P. Xu, "A CMOS Bandpass Sigma-Delta Modulator Employing SAW Resonator," in *Proc. IEE Intl. Conf. on Advanced A/D and D/A Conversion Techniques and Their Applications (ADDA' 05)*, July 2005, pp. 243-247.

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[6] R. Yu, Y.P. Xu, "A 65-dB DR 1-MHz BW 110-MHz IF Bandpass ΣΔ Modulator Employing Electromechanical Loop Filter," to be presented at *IEEE Custom Integrated Circuits Conf. (CICC'07)*, September 2007.

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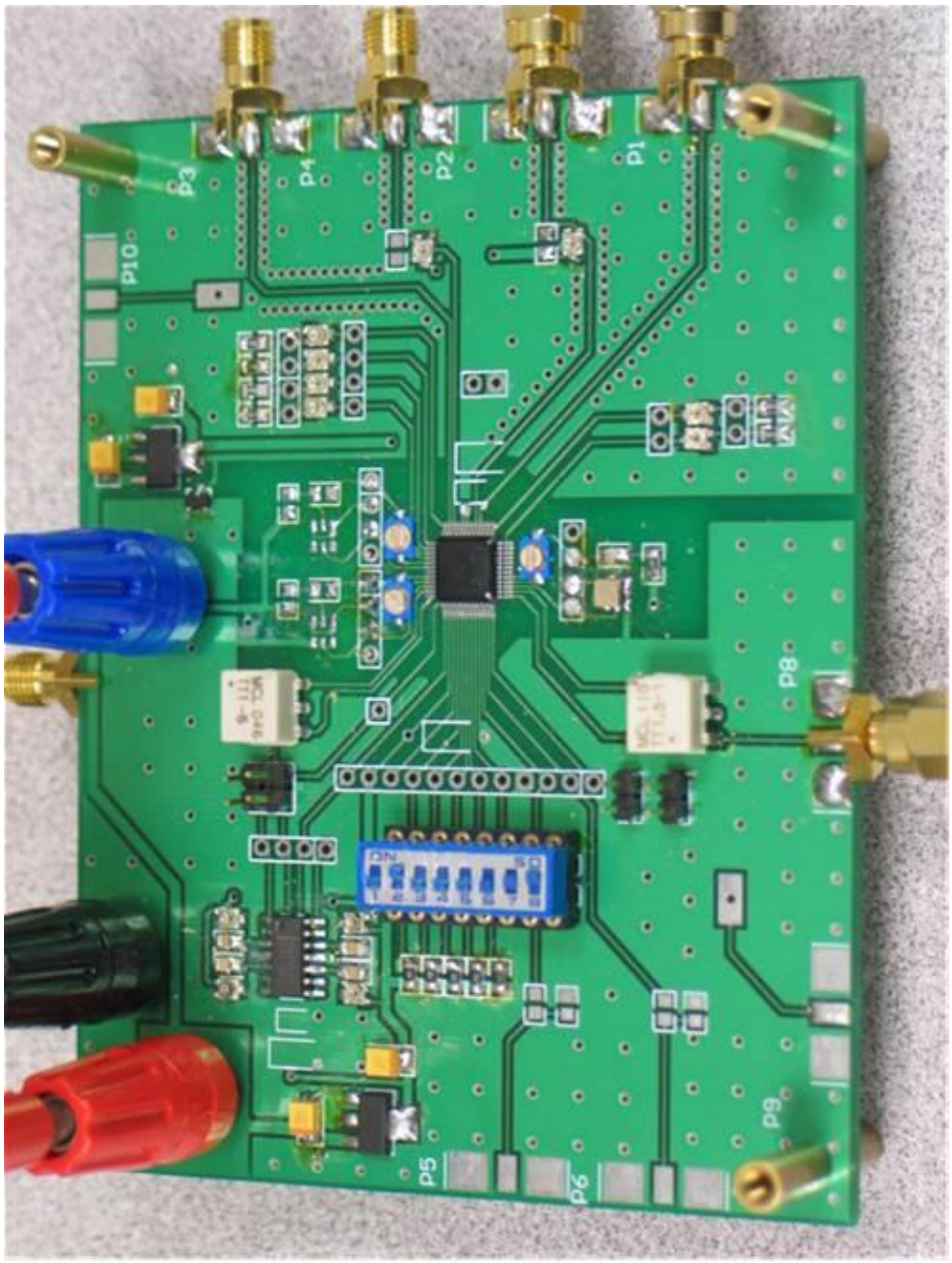
[9] One U.S. patent filed, serial number : 60/955,208, 2007.

APPENDIX B PHOTOGRAPHS OF TESING PCBS

B.1 PCB for the first-generation electromechanical resonator based 2nd-order bandpass ΣΔM

B.2 PCB for the second-generation electromechanical resonator based 2nd- and 4th-order bandpass ΣΔMs



A.3 PCB for the electromechanical filter based bandpass ΣΔM